Abstract—Power management has an ever increasing presence in the electronics industry due to the growth of battery powered mobile devices. The low-dropout voltage regulator (LDO) offers improved efficiency over other regulator topologies. However, the architecture suffers from stability issues, which usually necessitates a large off-chip capacitor to ensure the regulator's performance. This paper presents an alternative topology by removing the bulky external capacitor, thus allowing for greater power system integration. The proposed Current Amplifier Hybrid Compensation (CAHC) scheme implements an active feedback-feedforward compensation system and maintains both a fast transient response and full range alternating current (AC) stability from 0 to 50mA load currents even with a 100pF loading capacitance. The 1.2V External Capacitor-less LDO voltage regulator was designed and simulated in a commercial 0.35um CMOS technology, consuming only 61uA of quiescent current with a dropout voltage of less than 200mV. Simulated results demonstrate that the proposed External Capacitor-less LDO architecture overcomes the typical load transient and AC stability issues encountered in previous architectures. The combined size and component reduction of this architecture presents a more integrable and economic power management system.

Introduction

The widespread growth of mobile electronics in the past five years has increased the demand for efficient and compact power management circuits. In addition, power management is under increasingly tighter performance specifications as the market for these electronics continues to grow. The circuits in these portable electronics must operate with minimal power consumption creating a demand for low power solutions in a wide spectrum of applications. Additionally, low noise power supplies have become an integral part of today's portable applications because of the noise sensitive RF circuits that are used in portable electronics.

Low Drop-Out (LDO) voltage regulators are essential components of power management systems providing a constant voltage supply rails. These linear voltage regulators improve power efficiency by reducing the minimum voltage drop across the control device; this is accomplished by replacing the common-drain pass element is with a common-source configuration [6]. This decreased voltage overhead in the pass element results in less power dissipation, making this LDO regulator more suitable for low-voltage, low power, power management solutions.

While the LDO regulator has become popular due to its efficiency it requires control circuitry to ensure circuit stability. This paper describes the adaptation of the circuit compensation technique outlined by Milliken et al. in [5] to a three stage amplifier topology. A conventional LDO voltage regulator uses a relatively bulky output capacitor in the microfarad range with an equivalent series resistance (ESR) of a fraction of an ohm as shown in [6]. This dependence presents two problems. First, large microfarad capacitors cannot be realized in current design technologies. Therefore, existing LDO regulator designs utilize an external pin for a board mounted output capacitor. Second, the dominant pole is highly susceptible to variations in the frequency-dependent ESR. Leung and Mok propose an external capacitor-less LDO in overcoming this issue; however, the topology is unstable at low current loads and therefore unattractive for technological applications [2]. The topology outlined in this paper removes the external capacitor, minimizing board area and overall cost, while preserving stability under all loading conditions. The external capacitor-less circuit is also suitable for system-on-chip (SoC) designs as all components may be manufactured in silicon.

Removing the external output capacitor of a conventional LDO regulator greatly affects both transient and AC stability. Within the conventional topology, the output capacitor serves two purposes: it introduces a dominant pole in the AC response and provides an instantaneous source of charge during transient loading. A robust compensation scheme, therefore, is required to maintain circuit stability. The external capacitorless LDO regulator implements a fast transient path to stabilize the circuit in the absence of an output capacitor. Section II characterizes the uncompensated LDO regulator, including the pole locations and transient behavior. The proposed LDO architecture is described in Section III. The compensated 1.2V, 50mA capacitor-less LDO was simulated and the results are shown in Section IV and concluding remarks in Section V.

Uncompensated LDO

The most significant effects of removing the output compensation capacitor are the stability and transient performance degradation. The conventional LDO uses the large output capacitor to create a dominant pole and to provide an instantaneous charge source during loading transients. As the gates of the error amplifier are relatively slow, the LDO requires a fast transient path to suppress transient spikes.

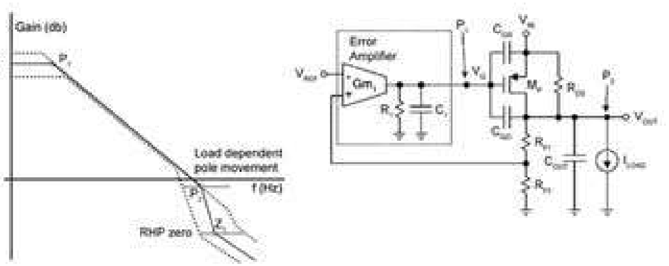

Fig. 1. LDO pole location and load dependent pole movement.

The two major poles of the uncompensated LDO are shown in **Fig. 1.** P1 is dominated by the output of the error amplifier and P2 is due to the load at the output. In order to minimize VDSAT of the pass element, the transistor is fairly large with a parasitic capacitance on the order of tens to hundreds of picofarads. CGD also forms a Miller capacitor, increasing the effective input capacitance of the stage by the gain of the pass element. This is typically 10 V/V at moderate load currents, but may be as large as 30 V/V as the circuit approaches no-load conditions. The large variation of the load current corresponds to a drastic change in the dominant pole location, from a few hertz to the tens of kilohertz range. Opening the loop, the location of P1 is given by

$$P_1 = \frac{1}{R\_1(C_1 + C_{GS} + A_{(pass)}C_{GD}}$$

where A_{pass} is the voltage gain of the pass transistor, M_P. P_1 resides at a relatively low frequency, in the kilohertz range. As Apass varies with operating conditions, mainly load current, P_1 is also load dependent. The second pole, P_2, is located at the LDO's output, as shown below:

$$P_2 = \frac{1}{C_{out}\left(R \| \frac{C_{GD}}{g_{mp}C_1 + C_{GS} + C_{GD}}\right)}$$

Where,

$$R = R_{DS} \| (R_{f1} + R_{f2}) \| R_{out}$$

As shown in Table I, the pass element's g_m and g_{RD} are sensitive to changes in load current. The parasitic capacitor, C_{GS}, is less load dependent at moderate loading but experiences a sudden drop under no load. A consequence of these dependencies is that, at low load currents, P_2 moves toward lower frequencies, as seen in **Fig. 1**. The largest change in parameter magnitude occurs from 0 to 5mA. The decrease in phase margin compromises loop stability at low and no-load conditions. Furthermore, the Miller capacitor C_{GS} introduces a parasitic, right-hand plane (RHP) zero, further reducing phase margin.

This RHP zero is usually ignored during conventional LDO regulator analysis, as it falls beyond the unity gain frequency. However, the zero may attract complex poles to the RHP, decreasing loop stability. The presented capacitorless LDO regulator requires a gain-bandwidth product of 1 MHz and at these frequencies the feedforward RHP zero has significant effects on stability at low load currents. The large external capacitor, C_{out}, used in conventional LDO regulators, improves the transient load regulation by delivering instantaneous current, allowing regulating loop time to react and provide the output current through the pass transistor. For a pulsed output current, the transfer of charge from the capacitor corresponds to a voltage drop at the output node. The removal of the capacitor results in the drastic charge depletion of the pass transistor as shown in **Fig. 2**.

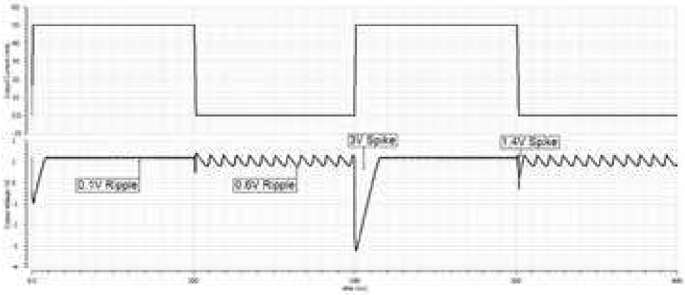

Fig. 2. Uncompensated LDO transient response to 0-50mA pulse (1us rise and fall time).

The rapid charge depletion results in large transient spikes and instability. The greatest spike occurs when the circuit is initially at no load conditions and the load current rapidly changes to I_{MAX}. In this case, the output voltage swing is modeled approximately as

$$\Delta V_{out} \approx \frac{I_{MAX} \Delta t}{C_{out}}$$

where Δt is the reaction time of the error amplifier loop. When the transient pulse exceeds the loop's bandwidth, the resulting voltage spikes can be very large. In absence of a large load capacitance, the reaction time of the loop should be minimized. The use of a fast feedforward path suppresses the large voltage spike by preventing charge depletion in the pass device.

Proposed LDO Architecture

The design of the external capacitor-less LDO regulator focused on, minimizing the overshoot and undershoot during transients, and improving the regulator's overall stability. Other goals included minimizing quiescent current draw and power consumption. LHP zeroes are introduced to achieve these goals. Previously, Miller amplifiers have been implemented to stabilize multistage amplifiers; however, this technique also generates a RHP zero [1]. A separate technique reported by Milliken is used here, as it eliminates the undesirable RHP zero [5].

I_D (mA)	g_m (mS)	g_{ds} (mS)	Gain (V/V)	C_{GS} (pF)	V_{OUT} (mV)
0.0	0.1	0.003	36.3	2.85	42.56
5.0	73.0	2.595	28.1	11.89	98.34
20.0	185.9	9.702	19.1	14.83	173.8
50.0	283.4	33.92	5.0	15.07	268.2

Table 1.

Since the capacitor-less LDO regulator does not have a large capacitor to create a dominant pole, it must be placed within the error amplifier. The overall pass transistor capacitance and output impedance convert current to voltage, introducing a propagation delay. The speed of the LDO is limited by this propagation delay which in turn is dependent on gm1, the error amplifier transconductance. As low power and low quiescent current are concerns, manipulation of gm1 is limited. A secondary path is necessary to provide the needed instantaneous current to the output node.

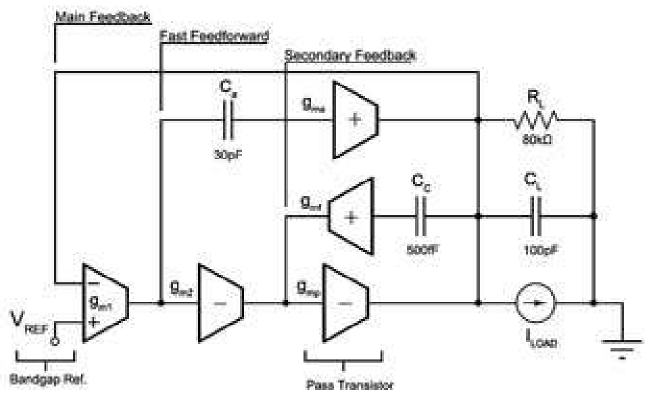

Fig. 3. Proposed LDO topology including fastfeedforward and secondary feedback networks.

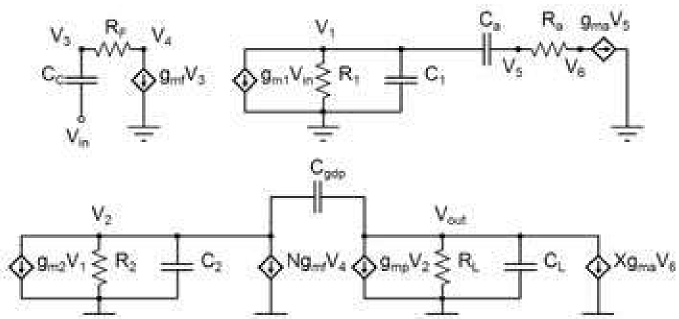

Fig. 4. Proposed LDO small signal model feedback networks.

A fast feedforward path as shown in **Fig. 3**, injects current directly into the output node via the coupling network. The path acts as a capacitive multiplier and presents a source of charge during load current steps. The load current step ΔI_{LOAD} is applied to the LDO, an output ripple ΔV_{OUT} is generated; the current flowing through C_a is extracted from C_{GD} until I_D, the pass transistor drain current, compensates ΔI_{LOAD} and pulls V_{OUT} back to steady state. The location of the poles and zeroes were obtained through symbolic computation via Maxima and can be simplified by extracting the first order terms yielding:

$$P_1 \approx \frac{1}{C_a R_1}$$

$$P_2 \approx \frac{1}{R_1 \left(C_L + C_{gdp} g_{mp} R_2 \right)}$$

$$P_3 \approx \frac{g_{ma} \left(C_L + C_{gdp} g_{mp} R_2 \right)}{g_{ma} R_2 C_L \left(C_{gdp} C_2 \right) + C_1 \left(C_L + C_{gdp} g_{mp} R_2 \right)}$$

$$P_4 \approx \frac{g_{ma} R_2 C_L \left(C_{gdp} C_2 \right) + C_1 \left(C_L + C_{gdp} g_{mp} R_2 \right)}{C_1 C_L R_2 \left(C_{gdp} + C_2 \right)}$$

$$P_5 \approx \frac{g_{mf}}{C_c}$$

$$Z_1 \approx \frac{g_{ma}}{C_a}$$

$$Z_2 \approx \frac{g_{m1} g_{m2} g_{mp}}{g_{ma} \left(g_{m1} g_{ma} R_a X \left(C_2 + C_{gdp} \right) + C_c g_{mf} g_{mp} R_f N \right)}$$

$$Z_3 \approx \frac{g_{ma} \left(g_{m1} g_{ma} R_a X \left(C_2 + C_{gdp} \right) + C_c g_{mf} g_{mp} R_f N \right)}{C_1 C_c g_{mf} g_{mp} R_f N}$$

$$Z_4 \approx \frac{g_{mp}}{C_{gdp}}$$

As expected, the feedforward network introduces a RHP zero, which may attract complex poles to the RHP, compromising stability. The secondary feedback, however, was designed to be unidirectional preventing such a zero and minimizing transient ringing. Strategic placement of the feed forward zeroes, Z_2 and Z_3, was achieved through the manipulation of gm_f and R_f and allowed for the cancellation of P_3 and P_4. This cancellation and the placement of P_5 at high frequency reduced the LDO to a two pole system. Z_4 was then placed well past the unity-gain frequency and was subsequently ignored.

Simulation Results

The proposed LDO design was verified in simulation with V_{ref} set to 1.20V, a maximum input voltage of 1.8V and 100pF load capacitance. The LDO was tested for load and line regulation, shown in Table II. Output voltage errors were less than 7:5% over the entire operating range. The regulator was then subjected to both 0–50mA and 50–0mA load transients with 1us rise and fall times. The 0–50mA transient exhibited a transient spike of 75mV and settled within 0.6us. Extracted parasitic capacitances produced 90mV of ringing in the 50–0mA transient – however this quickly subsided and a stable output was reached in < 10us in the worst case.

Turn-on settling time was found to be 0.6us and 3us for ±1% and ±0.1% respectively. The PSRR was simulated by applying a 1kHz sinusoidal input voltage and the gain was measured to be –52dB.

Parameter	[3]	[4]	[5]	[7]	This paper
Technology	0.35u CMOS	0.35u CMOS	0.35u CMOS	0.35u CMOS	0.35u CMOS
V_{IN} (V)	3.0	3.0–3.5	2.0	1.2	1.7
I_{MAX} (mA)	50	100	100	50	50
V_{OUT} (V)	2.8	3.3	1.8	1.0	1.2
I_Q (uA)	65	<3.3	54	95	<61
C_{LOAD} (pF)	100	0	100	20	100
VOUT (mV)	<90	550	<200	<150	<100
1% Settling Time (us)	<15 (0–50mA)	50 (0.1–100mA)	N/A	1 (0–50mA)	<0.6 (0–50mA)
PSRR (1kHz) (dB)	–57	–52.3	–64	N/A	–52
Loop Gain (dB)	55-62	N/A	42-110	50-57	72-92
Load Regulation (mV/mA)	0.56	N/A	0.003	0.28	0.0042
Line Regulation (mV/V)	<23	N/A	0.2	18	0.073

Table 2.

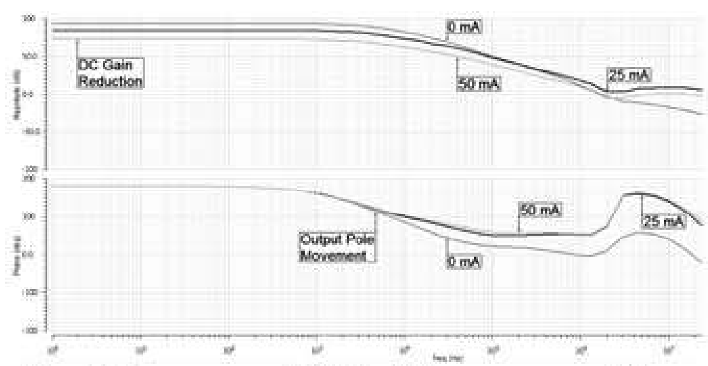

Fig. 5. Compensated LDO AC response at different load currents.

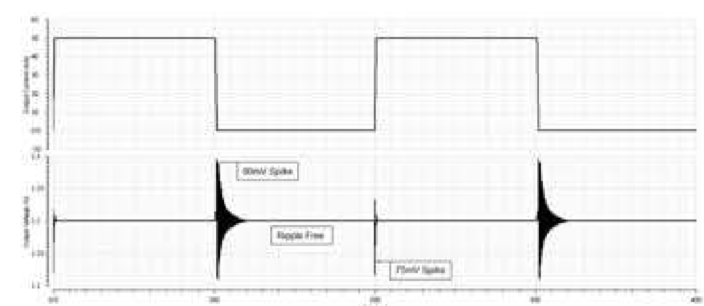

Fig. 6. Compensated LDO transient response 0–50–0mA pulse, 1us rise and fall time.

Conclusion

Simulated results demonstrate the viability of the proposed LDO architecture, which exceeds current work in the area of external capacitor-less regulators. In particular, this topology demonstrates both remarkable transient and AC responses and consumes only 61A of quiescent current. The small 30pF and 500fF capacitors may drive a load as large as 100pF. To further boost performance, an extra feedback network may be employed to allow for more accurate pole-zero placement. This additional precision would reduce settling time by prevent pole-zero doublet formation which lead to ringing. A comparison is made in Table II. In addition to consuming little power, the architecture provides superior settling times, load and line regulation. Fully integrated power management systems would benefit in terms of cost and silicon area the proposed LDO voltage regulator.

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