Model Predictive Critical Soft-Switching Enabling High-Performance Software-Defined Power Electronics: Converter Configuration, Efficiency, and Redundancy

Liwei Zhou

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Abstract

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Advanced power electronic techniques are crucial to enable high-performance energy conversion systems for the applications of various load and source interfaces, e.g., electric vehicle battery charger, solar power, wind power, motor traction, grid-connection. Also, the improvements on electrification for energy conversion contributes to the Carbon Neutrality with the reduction of fuel combustion. The control and design of the power conversion systems largely determine the efficiency, power density and system cost which typically need specialized design procedures. Since the types of interfaced energy sources may vary, the corresponding control algorithms and hardware configurations will be different. Thus, the power electronics system design is conventionally a specific routine based on the desired source and load requirements. Generally speaking, two main perspectives need to be considered when designing a power conversion system: (1) the power converter circuitry topology with the corresponding hardware components, e.g., low/high power circuits design, passive components design; (2) control algorithms and functions design, e.g., voltage/current control techniques, active/reactive power balancing and adjustment. However, the repetitive and specific power electronics design procedures for different load/source requirements are time-consuming and costly.

This thesis proposes a software-defined power electronics concept to develop a generalized auto-converter module (ACM) by leveraging variable-frequency critical-soft-switching, model pre-
dictive control techniques and high-performance litz-PCB inductors. The software-defined power electronics techniques can be applied to various types of electrified load/source applications without the need of repetitive hardware components and software algorithms designing procedures. The fundamental unit for the generalized concept, auto-converter module, is a type of MPC-based power module. A hierarchical control architecture is designed to manage the local ACMs and satisfy different load/source energy conversion requirements with high efficiency, high power-density and high-reconfigurability.

To achieve high-performance for the software-defined power electronics system, several advanced technologies are developed and integrated including variable-frequency critical-soft-switching, modular model predictive control, litz-PCB inductor design. Firstly, a variable-frequency critical-soft-switching technique is developed to adjust the switching frequency for the zero-voltage soft-switching. Doing so, the switching losses can be largely reduced with high efficiency. Secondly, the critical-soft-switching inductor is designed based on litz-PCB winding structure and neural network model to optimize the inductor losses and reduce the volume for the application of high frequency and large current ripple. Thirdly, a modular model predictive control method is designed for each of the local ACM to improve the dynamic performance and attenuate the oscillation caused by the variable frequency operation. Lastly, a hierarchical control architecture is developed to generalize the software-defined power electronics with multi-layer structure, central control layer, local module control layer and application layer. The hierarchical control architecture can be widely applied to different types of load/source interfaces, e.g., single/three-phase grid-connected inverters, motor traction inverter, battery charger, solar energy and so on. Leveraging the hierarchical control architecture and software-defined power electronics, the repetitive power converter hardware components and software algorithms design procedures can be simplified and standardized. Also, for different power converter applications, the efficiency and power density are both improved with better dynamic performance.
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Dedication

This thesis is dedicated to my mother, Yinhui Wu, my father, Chengtao Zhou, my paternal grandfather, Jianrong Zhou, my paternal grandmother, Guixin Li, my maternal grandfather, Minglue Wu and my maternal grandmother, Guangqing Liu, for their endless love and support throughout my life.
Chapter 1: Introduction

1.1 Background

The power electronics (PE) are widely applied in the electrified energy conversion systems ranged from low power chip level supplies, consumer electronics, middle power domestic compliance, server power supplies, to high power electric vehicle charger, solar energy, E-motor traction, wind power generation and so on. The power electronics techniques mainly focus on leveraging electronics knowledge to design and control the electric power conversion systems. With the increasing of global carbon dioxide emissions, the electrification of energy conversion system is attracting significant research interests. Especially in the transportation systems, the carbon dioxide generated by burning fossil fuels accounts for the majority of greenhouse gas (GHG) emissions. In the automobile industry, the traditional internal combustion engines are the main source of GHG emissions. The fuel burning efficiency is positively related to the degree of electrification in the automotive propulsion system as is shown in Fig. 1.1 [1]. From hybrid electric vehicle (HEV) to plug-in hybrid electric vehicle (PHEV) then to all-electric vehicle (BEV), the ratio of electrification is scaled up. Accordingly, the GHG emissions are reduced due to the improvement of fuel efficiency. Besides the attenuation of GHG emissions, the electric vehicles also have comfortable driving experience, intelligent autopilot techniques and safe propulsion system. Thus, the global electric vehicle stock is surging in the recent 10 years as is shown in Fig. 1.2 1. Power electronics techniques are crucial to the electrification of transportation since the EV battery charging/discharging, electric motor traction and automotive electronics system are all relying on the design and control techniques of PE. Besides the automobile industry, there are various applications in the electrified energy conversion systems that require power electronics, such as solar

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energy, wind power, grid-connected power supplies and so on is shown in Fig. 1.3(a). The main components of PE system is power converters to transform the electric power between alternate current (AC) and direct current (DC) formats. Four typical power converters include DC/DC converter, DC/AC inverter, AC/DC rectifier and AC/AC converter as is shown in Fig. 1.3(b). Thus, generally speaking, the PE techniques focus on the design and development of hardware/software based on the four types of power converters.

Power electronics design and development are typically specialized field for different types of electrified energy conversion systems. The design of the power electronics devices is always application-oriented since the requirements of different electrified load/source may vary. Thus, the corresponding hardware and software design will be diverse. Conventionally, to design a power converter, the specific parameter configuration requirement should firstly be comprehensively analyzed. On one hand, for the hardware part, the rated voltage/current/power requirements determine the device selection and PCB board design. The power converter topologies can also vary and are largely dependent on the interfaced load/source. Different types of interfaced load/source would also require disparate sensing circuits. On the other hand, for the software part, various types of applications need different number of sampling information, I/O channels, control function algorithms and so on. The different detailed configuration requirements of various industrial products make the power electronics design an application-oriented profession. The existing studies rarely focus on the generalization of the electrified energy conversion system.

The traditional power electronics design procedures can be generally summarized as five steps, converter configuration, hardware design, software/control design, experimental validation and standard compliance. Since the first step of power converter configuration depends on the interfaced load/source characteristics, rated input/output voltage/current level and power demands, the subsequent procedures will be largely diverse. A concept of power electronics building block (PEBB) has been proposed to standardize the hardware components for stackable energy conversion systems [2, 3, 4, 5, 6, 7, 8, 9, 10]. The PEBB concept is more focusing on the physical components design to generalize the hardware power modules with extensible voltage/current ca-
capacity. On the contrary, some studies have also developed power electronics control architectures in a high level perspective to cover various applications [11, 12, 13, 14, 15, 16]. Besides the generalized hardware and software control architecture designs for power electronics, some research developed modular concept for power converters to further generalize the power electronics de-

![Figure 1.1: Degree of electrification: typical fuel efficiency improvement and electric traction motor power.](image1)

![Figure 1.2: Global electric passenger car stock from 2010 to 2020.](image2)
Figure 1.3: (a) Different applications of power electronics and (c) the typical power converter structures.

sign procedures [17, 18, 19]. Other technical concepts studied the building of universal platform or infrastructure for the real-time power electronics testing and design [20, 21, 22].

1.2 Motivations

The typical power electronics design procedures are demonstrated in Fig. 1.4(a). Various types of applications are featured with different power converter, hardware and software control configurations. Thus, it is hard to generalize a universal design protocol that can cover all types of electrified energy load/source. The specificity of power electronics design is mainly reflected in the following three aspects.
Firstly, the characteristics of the interfaced loads/sources to the power converters are disparate. For example, the energy loads/sources can be divided into DC and AC. DC types of electric power include battery, solar energy, automotive 48-volt system and other low voltage power supplies. Among the DC electric power loads/sources, the required voltage/current or power control algorithms are different. Battery charging/discharging processes are typically featured with constant current (CC) and constant voltage (CV) control modes. The photo-electric effect in the solar energy system requires a maximum power point tracking (MPPT) technique to perform an optimal energy transformation efficiency. Grid-tied inversion systems demand a phase-locked loop (PLL) to synchronize the power converter with the grid frequency. Motor traction inverter of the electric vehicle needs to sample the rotor position for the speed and torque control.

Secondly, the difference of rated voltage and current configurations can lead to huge divergence
on the power converter and the corresponding sensor circuit design. The rated voltage/current values limit the selection of power switches for the tolerable maximum current/voltage across the switch. The sensor circuit design is also sensitive to the current/voltage ranges which could influence the sampling resolution and accuracy.

Thirdly, the time scales of the power electronics signals are different for various types of communicated information. The updating frequencies of the communication signals can be ranged from $ns$ to $min$ according to the control needs and micro-controller computation capability. For instance, the protection signals by detecting voltage/current samples may be iterated within $ns$ to $\mu s$. The voltage/current signals for power control purposes can be updated with the time periods from $\mu s$ to $ms$. Other grid service commands, user interfaced data monitoring may not require fast updating period which could be ranged from $ms$ to $s$.

Since the existence of the three aspects of specificity for the power electronics design, the power converters need to be specifically designed based on the demands. The targets for the power converters design mainly include high energy conversion efficiency, high power density, low cost to improve the energy conversion performance. In detail, the high efficiency means low power losses during the energy conversion processes. The high power density requests a high power level and low volume in the mean time. Low cost pursues less cost on the hardware components per volume of the energy conversion system.

Comprehensively considering the specificity feature of power electronics design and the target of improving the energy conversion performance, the dissertation develops a software-defined power electronics architecture to abstractly generalize the electrified energy conversion system and improve the energy conversion performance by leveraging advanced control, estimation algorithms and novel design techniques.

1.3 Contributions

The study of the dissertation develops a software-defined power electronics architecture by leveraging model predictive control (MPC), state estimation, variable-frequency critical-soft-switching
(VF-CSS) control algorithms and advanced inductor design techniques to abstractly generalize the energy conversion system with high performance.

- **Variable-Frequency Critical-Soft-Switching Control**: A VF-CSS method is developed by leveraging the variable-frequency controller to achieve critical-soft-switching operation of the power modules. The energy conversion efficiency is improved by 3% compared to the conventional fixed frequency hard switching.

- **High Performance Inductor Design Enabling Critical-Soft-Switching**: For the power module, the most crucial magnetic component of switch side inductor is designed based on litz type of PCB winding and optimal core structure to reduce the inductor losses, volume and cost. A neural network model is built to automatically analyze the litz type of PCB winding design for optimal configuration. The total inductor loss, volume and temperature rise are reduced by 4 times, 40% and 50°C compared to the existing commercial inductors.

- **Model Predictive Control for Modular Power Converters**: A modular model predictive control method is proposed to be combined with the variable-Frequency Critical-Soft-Switching Control for the improvement of dynamic performance, especially during transients. The extra oscillation caused by the variable frequency control can be attenuated by the MPC. Also, the developed MPC enhances the control bandwidth with higher reference tracking speed and less overshoot issue.

- **Hierarchical Software-Defined Control Architecture with MPC-Based Power Module**: A multi-layer software-defined power electronics architecture is designed based on the aforementioned VF-CSS and modular MPC to abstractly generalize the electrified energy conversion system. The proposed software-defined power electronics architecture is mainly featured with four merits: (1) generalized design procedures to reduce the repetitive power electronics design processes; (2) reconfigurable architecture to form different power converter topologies with the corresponding control functions; (3) wide application interfaces to be applicable for various types of electrified load/source; (4) redundant mechanism with
self-healing to diagnose and substitute the fault circuit components. Based on the generalized architecture, several design cases have been implemented experimentally including isolated/non-isolated DC/DC converter, grid-tied inverter, battery charger and motor traction inverter to validate the feasibility of the proposed concept.

- **High Efficiency and Power Density Grid-Tied Inverter Design**: A design case of high performance grid-tied inverter is developed based on the VF-CSS and modular MPC techniques to achieve high efficiency, power density and low cost. The VF-CSS contributes to an efficiency above 99% at the rated power of 15kW. A power density of 10.4kW/L is achieved based on the designed litz type of PCB inductor and above 1MHz switching frequency. The modified power module combined with a zero-sequence voltage control method enables non-isolated inverter topology with low leakage current and low cost.

- **MPC-Based Regulated Third Harmonic Injection for Zero-Sequence Stabilized LCL Inverter**: Another design case of regulated third harmonic injection (THI) method is developed based on MPC and zero-sequence-voltage stabilization of the modified LCL inverter topology to improve the DC bus utilization. Different from the conventional THI methods, the proposed technique implemented the third harmonic injection with MPC regulation in the zero-sequence frame. The robustness is improved with the MPC regulation. The THI distortion on the output side is bypassed by the modified power module. Also no extra optimization algorithms are needed to minimize the output THI distortion. The computation burden compared to the conventional THI method is reduced correspondingly.
Chapter 2: Variable-Frequency Critical-Soft-Switching for Modular Power Converters

Wide-bandgap devices (WBG) are attracting more and more attention in the field of power conversion system. Silicon carbide (SiC) and Gallium Nitride (GaN) MOSFETs are two types of semiconductor that have been widely used in industrial applications due to the superior characteristics in high power and high frequency behaviors [23], [24]. Applying wide-bandgap devices in power converters can achieve high switching frequency with high power level [25]. This characteristic could decrease the inductance/capacitance values to improve the power density [26]. One issue that should be carefully considered is the switching losses which are mainly caused by the overlapping voltage and current waveforms during turn-on and turn-off switching periods [27], [28]. The switching losses could be influenced by many factors such as the device intrinsic features, peripheral circuits, gate driver behavior, soft switching design, controlling strategy, etc [29]. For the generality point of view, an effective way to decrease the switching losses is by combining the last two parts: soft switching design and controlling strategy. Firstly, soft switching is a key technique to reduce the switching losses in power converters [30]. The principle of soft switching is to avoid the overlapping area of switch voltage and current waveforms [31]. It can be divided into zero-voltage soft switching (ZVS) and zero-current soft switching (ZCS). ZVS aims at minimizing the voltage across the switch during switching transients and ZCS deals with the switching tail current to minimize the losses during transient periods. To realize the soft switching operation, auxiliary circuits can be added to handle the turn-on and turn-off instants for switching losses minimization [32]. However, the active auxiliary circuits will induce more cost and controlling complexity. Another way to implement soft switching is by designing the passive component values, such as filtering inductance and capacitance, and power converter operating parameters, such
as current ripple, switching frequency, dead time, etc [33]. The passive soft switching methods could be implemented based on a common characteristic of the MOSFETs: turn-on losses of the most MOSFETs are much greater than the turn-off losses. So, the soft switching strategy can be designed to replace the higher turn-on losses with lower turn-off losses [34]. For the state of the art of passive soft switching techniques in DC/DC buck modules, the primary method is to enlarge the inductor current ripple with bidirectional flowing paths at peak/valley points. This operating mode can be implemented by synthesizing the filtering inductor design, switching frequency configuration, power rating requirement and MOSFET characteristic analysis. [35] studied the passive soft switching technique without adding active auxiliary circuit or passive snubbers and implemented the soft switching on a bidirectional three-phase paralleled buck converter to achieve high efficiency and power-density specifically in IGBT devices. [36] focused on the passive soft switching analysis for interleaved multi-phase DC/DC converter specifically in the application of energy storage systems. The current ripple balancing issue is studied for efficiency improvement. The aforementioned techniques have developed convincing methods to achieve ZVS operation. However, the transient performance of soft switching is another key topic that merits attention. A steadily fast control method can avoid the oscillation or overshoot issues during the dynamic period to further improve the soft switching losses. Specifically, the second part is the controlling strategy: a better controlling method can achieve superior dynamic performance and accurate tracking behavior. A fast and stable controller will cause less oscillation on the output waveforms which means the soft switching operation can be achieved accurately and maintained steadily, especially during the transient period. Thus, the switching losses induced by the hard switching will be decreased accordingly. The most commonly used controlling method is PI controller. It is simple to design and implement with good performance. However, the overshoot and dynamic oscillation issues are the main drawbacks due to the integral process. Another more advanced controlling method that has better dynamic performance is model predictive control (MPC) [37], [38]. It can generate the optimal input values for the system by predicting multiple steps based on the state space equations and cost function [39]. Compared to PI controller, MPC has been validated to have faster tracking
speed and better transient behavior if designed properly [40].

This chapter proposes a controlling method based on the above mentioned two aspects to improve the efficiency and power density of the DC/DC converter. Firstly, a critical soft switching method is designed to achieve the soft switching operation without auxiliary circuits. The boundary constraints of typical WBG devices are derived according to the dead time and peak/valley inductor currents. The controlling method is designed based on the critical soft switching boundary constraints. Then, the variable-switching constant-sampling frequency critical-soft-switching model-predictive-control (VSCS-MPC) method is proposed. For the general purpose, both the current source load and resistive load converters are validated with the proposed MPC method. The controlling method mainly includes two parts: frequency controller and MPC controller. Frequency controller is designed to reduce the switching losses of the converter under critical soft switching by controlling the inductor current ripple. The expected switching frequency is calculated according to the measured inductor current, output voltage and duty cycle. For the consideration of system stability to generate the PWM signals, the switching frequency are discretized into equally segmented bandwidth for the purpose of maintaining a constant sampling frequency. If the calculated frequency belongs to certain range of the bandwidth, a fixed switching frequency will be delivered to the PWM. And the MPC controller will receive the measured output voltage and inductor current to generate the optimal duty cycle for tracking the voltage/current references. In order to alleviate the calculation burden in high frequency application, an oversampling method is designed based on the segmented frequency controller. Specifically, the MPC, frequency controller and sampling will be updated based on a constant fundamental frequency, \( f_{\text{base}} \), and the PWM switching frequency will be determined by the discretized frequency controller according to the equally segmented bandwidth range. Thus, the switching frequency will be adjusted steadily at a certain integral multiple, \( n \), times of the fundamental frequency to achieve the soft switching operation when the calculated frequency is within certain bandwidth range. The system oscillation will be mitigated by avoiding a time-varying sampling frequency and instantaneously changed switching frequency. By combining the two controllers, the proposed VSCS-MPC can achieve
high efficiency and superior dynamic performance robustly. The analytical tests are implemented on a SiC testbench to verify the proposed controlling method.

2.1 Critical soft switching principles for DC/DC converter

In this section, the critical soft switching technique is introduced with the derived boundary conditions of dead time and peak/valley inductor current by datasheet and integral equations. The main purpose of the critical soft switching method is to replace the large turn-on loss of upper switch with small turn-off loss of lower switch [41], [42]. Fig. 2.1 shows the current paths of DC/DC converter during lower switch turn-off period. For the critical soft switching, a large current ripple is required to ensure negative valley inductor current to be lower than a threshold current level as is shown in Fig. 2.2. In the turn-off transient period of lower switch, the negative inductor current will discharge the upper switch output capacitor, $C_{os,m1}$. The ZVS of upper switch can be achieved if the $C_{os,m1}$ is fully discharged before it turns on. The ZVS operation

![Figure 2.1: The negative inductor current paths of DC/DC Buck converter.](image)

![Figure 2.2: Gate signals and inductor current for critical soft switching.](image)
depends on the interlock time between two switches and the value of inductor valley current. The inductor valley current is expressed as

\[ I_{L,\text{min}} = -I_{DS,M2} + I_{CDS,M1} - I_{CDS,M2}. \]  \hfill (2.1)

\( I_{DS,M1} \) and \( I_{DS,M2} \) are the drain current through the upper and lower switches, \( I_{CDS,M1} \) and \( I_{CDS,M2} \) are the current through the upper and lower switch output capacitance, respectively. Since

\[ I_{CDS,M1} = C_{DS,M1} \frac{dU_{DS,M1}}{dt} \]  \hfill (2.2)

\[ I_{CDS,M2} = C_{DS,M2} \frac{dU_{DS,M2}}{dt} \]  \hfill (2.3)

and \((U_{DS,M1} + U_{DS,M2})\) equals to the input source voltage, \( U_{\text{in}} \), which is a constant value, \( I_{L,\text{min}} \) could be expressed as

\[ I_{L,\text{min}} = -I_{DS,M2} - (C_{DS,M1} + C_{DS,M2}) \frac{dU_{DS,M2}}{dt}. \]  \hfill (2.4)

Similarly, the maximum positive value is

\[ I_{L,\text{max}} = I_{DS,M1} + (C_{DS,M1} + C_{DS,M2}) \frac{dU_{DS,M2}}{dt}. \]  \hfill (2.5)
The above current equations can be further analyzed by the integral calculation over interlock time, $T_d$, and drain-source voltage, $U_{ds}$, respectively, and expressed as

$$\int_0^{T_d} [I_{L,min} - I_{DS,M2}(t)] \, dt = Q_{min} = (2.6a)$$

$$\int_{U_{in}}^{T_d} -[C_{DS,M1}(U_{DS,M2}) + C_{DS,M2}(U_{DS,M2})] \, dU_{DS,M2}$$

$$\int_0^{T_d} [I_{L,max} - I_{DS,M1}(t)] \, dt = Q_{max} = (2.6b)$$

$$\int_{U_{in}}^{T_d} [C_{DS,M1}(U_{DS,M2}) + C_{DS,M2}(U_{DS,M2})] \, dU_{DS,M2}$$

where $Q_{min} \leq 0$ and $Q_{max} \geq 0$ are the total charge moved in the output capacitors. Assuming that $I_{ds}$ is varying linearly with time, the left side of the two equations in equation (2.6) can be calculated as

$$\int_0^{T_d} [I_{L,min} - I_{DS,M2}(t)] \, dt =$$

$$\int_0^{T_d} [I_{L,min} - (I_{L,min} - \frac{I_{L,min}}{T_d}t)] \, dt = \frac{1}{2}I_{L,min}T_d$$

$$\int_0^{T_d} [I_{L,max} - I_{DS,M1}(t)] \, dt =$$

$$\int_0^{T_d} [I_{L,max} - (I_{L,max} - \frac{I_{L,max}}{T_d}t)] \, dt = \frac{1}{2}I_{L,max}T_d.$$ (2.7b)

So, the critical soft switching can be achieved with the inequalities of $I_{L,min(L, max)}$ and $T_d$

$$\frac{1}{2}I_{L,min}T_d \leq Q_{min} \leq 0 \quad (2.8a)$$

$$\frac{1}{2}I_{L,max}T_d \geq Q_{max} \geq 0. \quad (2.8b)$$

Thus, the minimum negative and maximum positive inductor current can be derived with the variables of dead time, $T_d$, and the integration of output capacitors with drain-source voltages. The design of the converter should satisfy the two inequalities to guarantee the critical soft switching operation. The integral of switch output capacitance to drain-source voltages can be calculated
based on the datasheet provided by the device manufacturer. So the integrations of equation can be calculated by tracing several discrete voltage intervals multiplied by the corresponding capacitance value and then accumulating together. According to the relation waveform of switch output capacitance and drain-source voltage, the right side of inequalities (2.8) can be derived by tracing n points on the curve of switch output capacitance, $C_{oss}$, and summing up the n intervals together.

Then, the model of critical soft switching method can be expressed with the function image in Fig. 2.3. It can be shown that the blue regions are the feasible soft switching range according to the constraints of inequalities (2.8) with the maximum and minimum dead time requirement. Also, the soft switching ranges of typical GaN and SiC devices are given in Fig. 2.3. During controlling part in the following sections, the dead time and peak/valley inductor currents can be controlled within the critical soft switching region to reduce the switching losses with optimal frequency.

![Figure 2.3: The critical soft switching operation regions for different devices.](image-url)
2.2 Variable-switching constant-sampling frequency critical-soft-switching control

This section gives the detailed controlling method of the proposed variable-switching constant-sampling frequency critical-soft-switching model-predictive-control strategy. The VSCS-MPC includes two parts: frequency controller to achieve the critical soft switching operation; MPC controller to track the output voltage/current and improve the dynamic performance. The implementation of MPC controller has large computation burden. So, an explicit MPC method is applied to solve the optimization problem offline. And due to the characteristic of MPC, a fixed sampling time period is required. Thus, to combine the MPC and variable frequency controller, the switching frequency is equally segmented based on a fundamental frequency, $f_{s,\text{base}}$. The MPC and frequency controller is updated with $f_{s,\text{base}}$ to guarantee enough computation time. And the frequency controller will calculate the expected soft switching frequency and transfer it into a discrete value for PWM based on the pre-designed bandwidth ranges. Thus, the switching frequency for PWM is discretized to be $n$ times larger than the fundamental frequency, $f_{s,\text{base}}$, which avoids the oscillation of the time-varying switching frequency.

2.2.1 Frequency Controller

For the frequency controller, the main purpose is to operate the converter in critical soft switching region and reduce the switching losses. In every fundamental time period, the frequency controller receives the duty cycle and inductor current values from the MPC controller to calculate the desired switching frequency. Then, the switching frequency is discretized based on the bandwidth ranges to derive a fixed value for the PWM. The calculation of the switching frequency is based on the critical soft switching constraints which have been derived in section II. The design of the frequency controller includes the constraints and methodology which have been shown as following.
Constraints

The principle of the frequency controller is to generate the feasible switching frequency based on the critical soft switching boundary conditions. In every calculating period, the frequency controller receives the information of duty cycle and inductor current from the MPC controller. Then an expected switching frequency is pre-calculated for discretization based on the bandwidth ranges and send to the PWM module. During the calculation of the expected switching frequency, four parts of constraints need to be taken into consideration: critical soft switching threshold current, $I_{th}$, maximum device current, $I_{max}$, maximum thermal rising, $P_{thermal,max}$ and frequency ranges.

The constraints could be expressed as

$$I_{th} \leq I_{peak} = I_{L,ave} + \frac{\Delta i_L}{2} \leq I_{max}$$  \hspace{1cm} (2.9)

$$-I_{max} \leq I_{valley} = I_{L,ave} - \frac{\Delta i_L}{2} \leq -I_{th}$$  \hspace{1cm} (2.10)

$$P_{sw} + P_{con} \leq P_{thermal,max} = \frac{T_{j,max} - T_{case}}{R_{th,J-C}}$$  \hspace{1cm} (2.11)
\[ f_{sw,\text{min}} \leq f_{sw} \leq f_{sw,\text{max}} \]  

(2.12)

where \( I_{\text{peak}}, I_{\text{valley}}, T_{j,\text{max}}, T_{\text{case}} \) and \( R_{th,J-C} \) are the peak, valley points of inductor current, junction, case temperatures and thermal resistance, respectively. The inductor current ripple is the function of three variables, \( (I_{L,\text{ave}}, d, f_{sw}) \), and can be derived as

\[ \Delta i_L = \frac{d(1-d)U_{in}}{f_{s}L}. \]  

(2.13)

So the derived constraints (2.9)-(2.12) can also be expressed as the function of \( (I_{L,\text{ave}}, d, f_{sw}) \) with the help of the substitution in (2.13). Thus, the constraints of \( f_{sw} \) with respect to \( (I_{L,\text{ave}}, d) \) can be plotted in the 3D coordinate system as is shown in Fig.2.4 where the two surfaces represent the upper and lower limits of the frequency controller, respectively. The calculation of expected switching frequency is based on the boundaries of the constraints to mainly satisfy the critical soft switching.

**Methodology**

The operating trajectories of the frequency controller can be illustrated in Fig. 2.5. With the variation of inductor current and duty cycle, the maximum feasible frequency under the critical soft switching constraints can be derived by the function of \( f_{sw} \) with respect to \( (I_{L,\text{ave}}, d) \) (bold red lines in Fig. 2.5). Based on the derived critical soft switching boundary conditions, the maximum frequency controller trajectories are divided by positive/negative inductor current conditions and the expected switching frequency can be expressed as

\[ f_{s,\text{cal}} = \frac{(1-d)dU_{in}}{2(I_{L,\text{ave}} + I_{th})L}, \quad I_{L,\text{ave}} \geq 0 \]  

(2.14a)

\[ f_{s,\text{cal}} = \frac{(1-d)dU_{in}}{2(I_{th} - I_{L,\text{ave}})L}, \quad I_{L,\text{ave}} \leq 0 \]  

(2.14b)

where the threshold current of critical soft switching constraints, \( I_{th} \), is based on the results derived in the second section.
After the calculation of the expected switching frequency, the values are then discretized by a pre-designed bandwidth ranges which are the integral multiple of the fundamental frequency, $f_{s,\text{base}}$. The fundamental frequency for MPC and frequency controller is set to be 30kHz, thus the discretized frequency for PWM signals could be $n$ times of $f_{s,\text{base}}$. It should be noted that when a certain discrete bandwidth range of the switching frequency is derived, the integral multiple value of $n$ is rounded down to guarantee the soft switching is maintained by choosing a relatively lower switching frequency. The implementation of the frequency controller is shown in Fig. 2.6. Also, to make a better explanation of the discrete frequency controller, the function curve of calculated switching frequency with duty cycle is drawn in Fig. 2.7 under the rated current load. It can be seen that the vertical axis of the switching frequency is equally segmented with the bandwidth of 30kHz. The PWM frequency is discretized and assigned as the lowest value at each range of duty cycle. The relationship of PWM carrier signals and sampling signals are shown in Fig. 2.8 with a varying switching frequency from $4f_{s,\text{base}}$ to $f_{s,\text{base}}$.

2.2.2 Model Predictive Controller

MPC aims at tracking the output voltage/current according to the pre-defined references. In every calculating period of fundamental frequency, $f_{s,\text{base}}$, the MPC controller receives the measured inductor current, input/output voltage values and generates the optimal duty cycle for both
Figure 2.6: Discrete frequency controller with equally segmented bandwidth.

Figure 2.7: Equally segmented switching frequency with the function of duty cycle at the rated load current.
PWM module and frequency controller. The MPC formulations for both current source load and resistive load are shown in this section.

Firstly, the state equations of the DC/DC converter with LC filters and current source load can be expressed as

\[ i_L(k + 1) = i_L(k) - \frac{T_s}{L} u_o(k) + \frac{U_{in}T_s}{L} d(k) \]  

\[ u_o(k + 1) = \frac{T_s}{C} i_L(k) + u_o(k) - \frac{T_s}{C} i_o(k). \]

(2.15a)  

(2.15b)

For the resistive load, the term \( i_o(k) \) in (2.15) can be replaced with \( u_o(t)/R_{load} \) and \( u_o(k)/R_{load} \), respectively, where \( R_{load} \) is the output resistor. For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the input voltage during test, the last term of (2.15), \( U_{in} d(k) \), can be replaced by the phase leg output voltage, \( u_x(k) \). The state-space model

![Figure 2.8: Variable PWM carrier signals and constant sampling signals of the VCS-MPC method.](image)

Figure 2.8: Variable PWM carrier signals and constant sampling signals of the VCS-MPC method.
with current source load are in standard matrix format of

\[ X_{k+1} = A_i X_k + B_i u_{ik}, \]

(2.16a)

\[ A_i = \begin{bmatrix} 1 & -\frac{T_i}{T} \\ \frac{T_i}{C} & 1 \end{bmatrix}, \quad B_i = \begin{bmatrix} \frac{T_i}{T} & 0 \\ 0 & -\frac{T_i}{C} \end{bmatrix}, \]

(2.16b)

\[ X_k = \begin{bmatrix} i_L(k) \\ u_o(k) \end{bmatrix}, \quad u_{ik} = \begin{bmatrix} U_{in}(k) \\ i_o(k) \end{bmatrix}. \]

(2.16c)

The state-space model with resistive load is

\[ X_{k+1} = A_r X_k + B_r u_{rk}, \]

(2.17a)

\[ A_r = \begin{bmatrix} 1 & -\frac{T_r}{T} \\ \frac{T_r}{C} & 1 - \frac{T_r}{RC} \end{bmatrix}, \quad B_r = \begin{bmatrix} \frac{T_r}{T} \\ 0 \end{bmatrix}, \]

(2.17b)

\[ X_k = \begin{bmatrix} i_L(k) \\ u_o(k) \end{bmatrix}, \quad u_{rk} = \begin{bmatrix} U_{in}(k) \end{bmatrix}. \]

(2.17c)

To derive the state matrix for MPC formulation, the output current is regarded as the input variable. So, in the implementation of the control, the current load can be measured and adjusted as a constraints for the input vector. In the standardized state matrix, the voltage/current references can be defined as \( \tilde{X} \) and the tracking errors between the measurement and the references are expressed as \( \tilde{X} \) which are composed of

\[ \tilde{X}_k = \begin{bmatrix} i_{Lr} \\ u_{or} \end{bmatrix}, \quad \tilde{X}_k = \begin{bmatrix} i_{Lr} - i_L(k) \\ u_{or} - u(k) \end{bmatrix}. \]

(2.18)

Thus, the cost function includes two terms

\[ \min \sum_{k=0}^{N_c} \tilde{X}_k^T Q \tilde{X}_k + \sum_{k=0}^{N_p-1} \Delta u_k^T R \Delta u_k. \]

(2.19)
For the penalties of the cost function, $Q$ and $R$ represent the weighing factor matrices that are implemented on the state values and input values, respectively. For the state value part, more weight is addressed on output voltage in current source load converter because the inductor current is restricted by the current load. For the input value part, more weight is addressed on duty cycle to stabilize the system behavior. Typical values for $Q$ and $R$ are $[1, 0; 0, 1000]$ and $[1000, 0; 0, 1]$, respectively. The constraints of the MPC controller can be expressed as

$$\hat{X}_{k+1} = A\hat{X}_k + Bu_k \in X$$  \hspace{1cm} (2.20)
\[
\Delta u_k = u_k - u_{k-1} \in \mathcal{U}
\]  
\[\begin{bmatrix}
-I_{L,max} \\
0
\end{bmatrix} \leq X_k \leq \begin{bmatrix}
I_{L,max} \\
U_{in}
\end{bmatrix}.
\]  
(2.21)  
(2.22)

With current source load, the input constraint is

\[\begin{bmatrix}
0 \\
i_o(k)
\end{bmatrix} \leq u_{ik} \leq \begin{bmatrix}
U_{in} \\
i_o(k)
\end{bmatrix}.
\]  
(2.23)

Figure 2.11: Proposed variable-switching constant-sampling frequency critical-soft-switching Model-predictive control diagram.

Figure 2.12: The waveforms of PWM carriers and trigger of the sampling and control.
The second term of \( u_{ik} \) is the output current from the known current source load. The controller assigns the measured value by setting the constraints as is shown in (2.23). This configuration allows a real-time adjustment of the output current that is compatible with explicit MPC. With resistive loads, the input constraint is simplified as

\[
\begin{bmatrix} 0 \end{bmatrix} \leq u_{rk} \leq \begin{bmatrix} U_{in} \end{bmatrix}.
\]

(2.24)

To achieve a high frequency for the DC/DC converter and reduce the calculation load of the controller, the MPC problem is solved explicitly by generating a piecewise affine feedback law [43]. Fig. 2.9 shows the mechanism of explicit MPC implementation process. The state model and constraints of the dynamic system are built offline to generate an online search tree and feedback law for optimization. In each controlling time period, the active region, \( r \), is searched with the matrices \( H_r \) and \( K_r \). Then, in each of the specific active region, the corresponding feedback law matrices, \( F_r \) and \( G_r \), are applied to calculate the optimal input values with the prediction horizon. Only the first value of the input matrix is applied to the dynamic system for MPC control.

In every fundamental time period, the pre-designed search tree can find the optimal duty cycle based on the updated state values of inductor current/output voltage. Explicit MPC avoids the time-consuming online optimization process, thus it is suitable for high frequency control. A generated piecewise affine region block with one input variable of phase leg output voltage, \( u_x \), and two state variables of output voltage, \( u_o \), and inductor current, \( i_L \), are shown in Fig. 2.10 with a prediction horizon of 5. Based on the implementing process of Fig. 2.9, the colored areas represent the \( n \) regions for MPC to search and optimize according to the feedback law. Specifically, the matrices \( H_r \) and \( K_r \) will lead to an active region. The matrices \( F_r \) and \( G_r \) will help calculate the optimal duty cycle for the PWM signals.

The whole controlling diagram of VSCS-MPC is shown in Fig. 2.11. At each sampling period of \( T_{s,base} \), the frequency controller receives the measurement of inductor current from ADC and duty cycle from MPC controller. The discretized frequency (\( n \) times of \( f_{s,base} \)) will be generated
from the frequency controller and delivered to update the carrier for the PWM signals. This mechanism will guarantee the consistency of sampling, triggering of the control and updating of the PWM. Thus, the discrete frequency bandwidth could avoid a time-varying switching frequency and improve the system stability. Specifically, an example of the discrete frequency controller to trigger the sampling and control is shown in Fig. 2.12. It can be seen that the PWM frequency is 6 times greater than the fundamental frequency.

Table 2.1: System Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>100-200 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>0-200 V</td>
</tr>
<tr>
<td>Output current</td>
<td>0-20 A</td>
</tr>
<tr>
<td>Resistive load</td>
<td>11 Ω</td>
</tr>
<tr>
<td>Capacitor</td>
<td>36 μF</td>
</tr>
<tr>
<td>Inductor</td>
<td>20, 110 μH</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>10-100 kHz</td>
</tr>
</tbody>
</table>
Figure 2.15: Inductor current and output voltage waveforms with output voltage reference step from 100V to 120V based on VSCS-MPC of current load.

Figure 2.16: (a) Inductor current, output voltage and (b) zoomed waveforms with output voltage reference step from 100V to 80V based on VSCS-MPC of current load.

Figure 2.17: (a) Inductor current, output voltage and (b) zoomed waveforms with inductor current reference step from 5A to 8A based on VSCS-MPC of resistive load.
Figure 2.18: (a) Inductor current, output voltage and (b) zoomed waveforms with inductor current reference step from 8A to 5A based on VSCS-MPC of resistive load.

Figure 2.19: (a) Inductor current, output voltage and (b) zoomed waveforms with output voltage reference step from 50V to 80V based on VSCS-MPC of resistive load.

Figure 2.20: (a) Inductor current, output voltage and (b) zoomed waveforms with output voltage reference step from 80V to 50V based on VSCS-MPC of resistive load.
Figure 2.21: (a) Inductor current, output voltage and (b) zoomed waveforms with output voltage reference step from 100V to 120V based on PI controller.

Figure 2.22: (a) Inductor current, output voltage and (b) zoomed waveforms with output voltage reference step from 100V to 80V based on PI controller.

Figure 2.23: VCS-S-MPC of resistive load: (a) output voltage, inductor current, output current experimental and (b) zoomed waveforms with inductor current reference step from 1A to 4A.
Figure 2.24: VSCS-MPC of resistive load: (a) output voltage, inductor current, output current experimental and (b) zoomed waveforms with inductor current reference step from 4A to 1A.

Figure 2.25: VSCS-MPC of resistive load: (a) output voltage, inductor current, output current experimental and (b) zoomed waveforms with inductor current reference step from 6A to 9A.

Figure 2.26: VSCS-MPC of resistive load: (a) Output voltage, inductor current, output current experimental and (b) zoomed waveforms with inductor current reference step from 9A to 6A.
Figure 2.27: VSCS-MPC of resistive load: (a) Output voltage, inductor current, output current experimental and (b) zoomed waveforms with output voltage reference step from 50V to 80V.

Figure 2.28: VSCS-MPC of resistive load: (a) output voltage, inductor current, output current experimental and (b) zoomed waveforms with output voltage reference step from 80V to 50V.

Figure 2.29: PI of resistive load: (a) output voltage, inductor current, output current experimental and (b) zoomed waveforms with output voltage reference step from 50V to 80V.
Figure 2.30: PI of resistive load: (a) output voltage, inductor current, output current experimental and (b) zoomed waveforms with output voltage reference step from 80V to 50V.

Figure 2.31: Soft switching performance of upper switch during turn-on and turn-off transients.

Figure 2.32: Testbench of multi-phase DC/DC converter.
2.3 Results

Analytical tests are implemented to verify the proposed controlling method. The simulated and experimental waveforms of VSCS-MPC and PI results are shown in this section to verify the better dynamic performance of MPC in maintaining the soft switching operation. Firstly, the VSCS-MPC is tested with current source load. And the simulation results are shown in Fig. 2.13 to Fig. 2.22.
The parameters of the converter are: \( L=20\mu H, C=36\mu F, \text{load}=5-20A, U_{in}=100-200V, u_o=0-200V. \) And the switching frequency ranges are 30k-600kHz. The MPT tool box is used for generating the piece wise affine search tree [44]. Fig. 2.13 and Fig. 2.14 show the inductor currents and output voltages with the current load variations from 10A to 15A and 15A to 10A, respectively. From the zoomed inductor waveforms, it can be seen that the critical soft switching operation is maintained during the transient period since the ripple currents are remained negative for soft switching turning on the upper switch. Fig. 2.15 and Fig. 2.16 show the inductor currents and output voltages with the output voltage reference variations from 100V to 120V and 100V to 80V, respectively. Also the zoomed inductor waveforms show that the critical soft switching operation can be maintained during the transient period.

Besides the current source load, the resistive load case is also verified with simulated and experimental tests. As is shown in Table 2.1, the parameters of the converter are: \( L=110\mu H, C=36\mu F, \text{load}=1-10A, U_{in}=100-200V, u_o=0-200V. \) And the switching frequency ranges are 10k-100kHz with 10kHz of fundamental frequency. Fig. 2.17 to Fig. 2.20 show the simulated results of inductor current control and output voltage control with VSCS-MPC. Fig. 2.23 to Fig. 2.28 represent the experimental results of inductor current and output voltage control under various testing conditions. For the inductor current control, Fig. 2.17 and Fig. 2.18 show the inductor current reference steps from 5A to 8A and 8A to 5A in simulation. And Fig. 2.23, 2.24, 2.25, 2.26 give the experimental results of inductor current reference step from 1A to 4A, 4A to 1A, 6A to 9A and 9A to 6A, respectively. For the output voltage control, Fig. 2.19 and Fig. 2.20 show the output voltage reference steps from 50V to 80V and 80V to 50V in simulation. Fig. 2.27 and Fig. 2.28 represent the output voltage reference steps from 50V to 80V and 80V to 50V, experimentally.

Besides the proposed VSCS-MPC results, the traditional PI controlling method is also tested for comparison. Fig. 2.21 and Fig. 2.22 show the simulated results of output voltage reference steps from 100V to 120V and 100V to 80V with PI controller. Fig. 2.29 and Fig. 2.30 represent the experimental results of output voltage reference steps from 50V to 80V and 80V to 50V with PI controller.
It can be seen from the VSCS-MPC and PI comparison that there exists oscillation during the transient period of PI results which means the soft switching is lost. Thus, more hard switching losses will be generated. Also, the dynamic period of VSCS-MPC is shorter than the PI method. The transient period of VSCS-MPC is 0.4ms to track the references while PI is 1.8ms. And the overshoot of PI in transient is higher than VSCS-MPC. The typical soft switching performance of the upper switch is captured with drain-source voltage and gate-source voltage. The turn-on and turn-off periods in Fig. 2.31 show that the upper switch is zero voltage turned on. The test bench is shown in Fig. 2.32 for the validation of the proposed controlling method. The hardware is designed as a three-phase power converter. Each phase has 2×Wolfspeed C2M0025120D SiC devices with 25mΩ $R_{ds, on}$, 2×gate drivers, one phase leg output current sensor. Also, for testing DC/DC with LC filter, a component board is connected between the converter board and the load. It includes three phase capacitors, 3 capacitor output voltage sensors and 3 output current sensors. And the resistive load is composed of three paralleled power resistors, TE1500B33RJ. Each has 33Ω, 1.5kW. Finally, the efficiency curve comparison between critical soft switching and hard switching is drawn in Fig. 2.33. It can be seen that with the proposed VSCS-MPC method, the efficiency of the DC/DC converter can reach up to 99%. For further detailed analysis, the comparison of break down switching loss distribution between soft switching and hard switching is shown in Fig. 2.34. It can be seen the turn-on loss is much larger than other types of switching losses and dominates the hard switching which could be avoided by soft switching.

### 2.4 Summary

This chapter develops a VSCS-MPC method for DC/DC converter. The critical soft switching boundary conditions are derived. The switching losses are reduced under critical soft switching operation through discrete frequency controller. An equally segmented frequency bandwidth range is designed to steadily adjust the switching frequency with constant sampling period. The system stability is improved due to a fixed sampling frequency. Explicit MPC controller is designed for tracking the output voltage/current. Because of the fast response and better dynamic behavior of
MPC, the hard switching is avoided during transient period compared to the traditional PI controller and the efficiency is further improved. The system volume is reduced with small inductor by applying a high switching frequency.
Chapter 3: High Performance Inductor Design Enabling

Critical-Soft-Switching

Electrified energy conversion systems especially for the electric vehicle and more electric airplane systems are developing towards the directions of higher power density, higher efficiency and lower cost. The key components of DC/DC and DC/AC power converters need to be carefully designed to achieve the goals. A promising method to increase the power density while reducing the losses is by leveraging the critical soft switching technique. It permits to increase switching frequency by a factor of 5 and reduce the required inductance by a factor of 20. Thus, the volume of filtering components can be decreased. However, a large current ripple is required for achieving critical soft switching operation with high frequency. Thus, the inductor needs to be carefully designed to handle large current ripple for the critical soft switching.

Inductor has been playing an essential role in the energy conversion system of DC/DC and DC/AC power converters to filter out the switching-frequency ripple. In a power converter circuit, the inductor accounts for a significant part of the total power losses. Especially for the application of high power, high frequency power converters with critical soft switching operation of large current ripple, the system efficiency is highly related to the electromagnetic performance of the inductor. Also, the volume of the inductor is crucial to the power density of the energy conversion system. Thus, the design and optimization of inductor for critical soft switching contributes to the efficiency and power density of the power converter.

Many references have studied and summarized the magnetic design procedures for power converters [45], [46], [47]. Also some advanced methods such as the Artificial Neural Network (ANN) [48], [49] or Fuzzy Logic [50] algorithms have been developed. However, there exist deviations between the theoretical analysis and assembled prototypes, especially in the high frequency/high
power applications. The deviations are mainly caused by two factors. First is the structure and spatial layout differences of the core/coil. The topology of the core, winding method of the coil and even the distance among the conductors will bring differences on the performance of the inductor, such as inductance, flux density, copper/core losses, etc [51], [52]. Second is the high frequency electromagnetic behaviors of the coil excited by a high current ripple in the conductor. A high frequency current excitation will result in significant AC losses which may dominate the whole copper losses. This AC losses are caused by the skin and proximity effects of the conductors and are difficult to analyze theoretically [53]. This chapter focuses on the structural optimization of core and coil to reduce the volume, cost and total losses especially considering the high frequency copper losses which is barely mentioned in many of the inductor design references.

For the evaluation of inductor design, some key aspects need to be carefully considered such as the efficiency, volume, fabrication and cost. Firstly, for the efficiency, the inductor losses are mainly composed of core and copper losses. The core losses are caused by the alternating magnetization in a magnetic core which include hysteresis loss and eddy current loss [54]. The selection of core material influences the core losses. Ferrite core is a desired option for high frequency inductor design considering its low power loss density. Due to the large permeability, the air-gap is commonly added for a ferrite core to avoid saturation. Based on the targeted frequency range of 100kHz to 1MHz, ferrite core is selected for the core structure design. The copper losses are induced by the equivalent resistance of the winding. Using thicker winding could reduce the resistivity of the conductor. Thus the DC copper losses will be reduced. However for the high frequency current excitations, the skin and proximity effects will result in significant AC losses. The litz type of conductor could be adopted for reducing the AC losses by winding multiple strands of conductors in parallel [55, 56, 57, 58, 59, 26]. Specifically, [55] and [56] analyze the litz and solid types of round wire for the inductor thermal behavior. A preliminary litz PCB winding model was designed in [57] to reduce the AC resistance. [58] and [59] designed two-layer litz PCB inductors for domestic induction heating and wireless charging coil, respectively. However, multi-layer (>2) litz PCB winding has not been studied in depth which is addressed in this chapter for a better AC
resistance reduction. Secondly, for the consideration of volume and fabrication, different structures of the core are suitable for various winding method. Considering the PCB winding’s convenience for manufacturing, fabrication and high space utilization, E cores with PCB windings can combine dense designs that can be mass-produced. Thirdly, for the cost, the litz wire cost more than the normal solid wire. However, if PCB is applied for the winding fabrication, the cost will be largely reduced when demanding a mass-production. So, this chapter developed a litz type of PCB 3D layout to apply the litz conductor in PCB winding.

This chapter is arranged as following. First part is the theoretical design procedures of inductor optimization. High current ripple/switching frequency requirements of critical soft switching are illustrated to specify the targeted application of the design. An iterative optimization method is developed to find the optimal number of turns, air-gap with the desired operating range of frequency for the reduction of total losses. The theoretical analysis will provide the guideline of structural inductor design. Second part is the structural design of core and coil. Based on the analysis in first part, the specific structures of core and coil are further optimized. For the coil, the high frequency AC losses are analyzed with the skin and proximity effects. A 3D litz PCB routing method is developed to emulate the twisted litz wire for the reduction of AC resistance. The ratio of AC to DC resistance, space utilization between multi-layer litz PCB and solid PCB are analyzed in detail. For the core, four types of core structure, E-E, E-I, I-I, E-Air (E-A) are developed based on the window/air-gap space and PCB winding parallelization. The trade-off of different core structures is illustrated with the combination of litz/solid PCB winding. Two 4-layer neural-network models are designed to analyze the AC resistance factor of the proposed solid/litz PCB winding. A generalized PCB-based inductor design method is developed leveraging the neural network model to reduce the losses. Finally, depending on the theoretical and structural design of core and coil, ten prototypes are finalized with different combination of E-E/E-I/I-I/E-Air cores and litz/solid PCB windings. The finalized prototypes are emphasized on different merits of the key factors for inductor design, such as losses, volume and cost, which could provide practical references for industrial inductor design with various trade off requirements. The experimental results verify the theoretical
and structural analysis.

3.1 Theoretical Design

The designed inductor is targeted for critical soft switching converter operating at a high current ripple. The main purpose of the critical soft switching technique is to reduce the total switching losses by replacing the large turn-on loss of upper switch with small turn-off loss of lower switch. Critical soft switching permits to increase switching frequency by a factor of 5, and reduce the required inductance by a factor of 20. For the total losses of a non-isolated power converter, as is shown in Fig. 3.1(a) of a DC/DC converter or Fig. 3.1(b) of a three-phase DC/AC converter, the high current ripple inductor losses on the switch side account for a significant part of the power conversion losses. The critical soft switching method could be applied by adjusting the current ripple to certain values which requires the inductance to be designed within a certain range [30], [42], [60]. So the critical soft switching parameters and loss optimization for inductor design are performed in this section theoretically.

3.1.1 Critical Soft Switching Parameters

In a buck module of Fig. 3.1(a), the turn-on losses are much higher than the turn-off losses. A critical soft switching technique could be implemented to replace the large turn-on losses of the upper switch with small turn-off losses of the lower switch. The principle is to enlarge the current ripple on the inductor and make sure the peak/valley points of the inductor current is beyond certain threshold. Thus the current direction of the inductor is bidirectional and the soft switching turn-on of both switches will be guaranteed [61]. The soft switching waveforms during switching transient are illustrated in Fig. 3.2. Also, the soft switching turn-on transient of upper switch is shown in Fig. 3.1(a).

A negative current from the inductor is expected to fully discharge the output capacitor of upper switch before it is turned on [61]. Thus the large turn-on losses will be minimized by soft switching. So, the critical soft switching requirements of inductor current are
In the inductor design perspective of soft switching, the current ripple is the key parameter that will influence the inductance. And the soft switching requirements of peak/valley inductor currents limit the range of current ripple. For a general design application, both AC (60Hz) and DC currents are taken into consideration for the peak/valley inductor currents requirements of soft switching. The current ripple is the function of switching frequency, inductance and DC voltage

\[ \Delta i_L = \frac{d(1-d)U_{in}}{f_s L}. \]  

(3.3)
For DC current, the maximum inductance for soft switching can be derived accordingly as:

\[ L_{\text{max,DC}} = \min_{d_{\text{min}} \leq d \leq d_{\text{max}}} \frac{d(1 - d)U_{\text{in}}}{2([I_{\text{L,ave}}] + I_{\text{threshold}}) f_s}. \]  

(3.4)

For AC current, the most critical soft switching operating points of sinusoidal waveforms are the peak/valley points. The maximum inductance requirement is:

\[ L_{\text{max,AC}} = \min_{d_{\text{min}} \leq d \leq d_{\text{max}}} \frac{d(1 - d)U_{\text{in}}}{2(\sqrt{2}|I_{\text{L, rms}}| + I_{\text{threshold}}) f_s}. \]  

(3.5)

According to equation (3.3), the switch side inductor current ripple is largely determined by the DC bus voltage. For the DC/DC converters in Fig. 3.1(a), the input and output voltage levels can be selected arbitrarily with the desired power and voltage requirements. However, for the three-phase DC/AC converter in Fig. 3.1(b), the DC bus voltage is generally depending on the grid voltage. The typical three-phase grid voltage for the US is line-to-line 480\(V_{L-L}\) which is line-to-neutral 277\(V_{L-N}\). And the DC side voltage should be at least twice higher than the AC grid voltage amplitude which is 783V. Since it is common to configure the DC voltage 10% higher than the AC voltage limit to avoid duty cycle saturation issue, we designed the DC bus voltage as 850V. For the current rating of switch side inductor design, a high power DC/AC converter power module with rated power of 11-13kW requires 16\(A_{\text{RMS}}\). And based on equation (3.5), the required maximum ripple current for the designed inductor to handle is 50A. And for the selection of winding gauge under soft switching operation, the equivalent RMS of current ripple is lower than 30A based on the relationship of triangular current ripple peak-to-peak value, \(I_{\text{rms,triangle}}\), and RMS value, \(I_{\text{rms,triangle}}\): \(I_{\text{rms,triangle}} = I_{p-p,\text{triangle}}/\sqrt{3}\). Thus, a gauge 8 wire is capable of handling 40A at 60 °C according to the AWG Table.

3.1.2 Iterative Optimization

The iterative optimization is based on the soft switching parameters of current ripple, minimum requirement of inductance, voltage level and power ratings for specific switching frequency. An
inductor design optimization method is developed in this section to iteratively sweep the switching frequency and number of turns for finding the optimal inductor parameters. The theoretical analysis of the design procedure includes the core selection, coil design, air-gap adjustment and iterative searching for switching frequency and turn number.

Core selection

The core of the inductor is an essential part that is functioned for magnetization at specific frequency. The performance of the inductor is largely influenced by the core size and structure. Some key factors need to be considered for the selection of core: the core losses (including the hysteresis losses and the eddy current losses), the flux density saturation issues, the area product (AP) power capability checking.

The core size could be designed based on the AP power capability checking method [46]. The AP checking method has been developed to evaluate the power capability of the core based on the comparison of two values: electrical requirements of current and flux density, geometrical capability of the core, respectively. The electrical requirement, \( AP_e \) is related to the inductance, \( L \), peak current, \( I_{pk} \), peak flux density, \( B_{pk} \), current density, \( J_{rms} \), window utilization factor, \( K_u \) and can be expressed as

\[
AP_e = \frac{L I_{pk}^2 10^4}{B_{pk} J_{rms} K_u}.
\]  

(3.6)

The geometrical capability of the core, \( AP_g \) is defined as the product of window area, \( W_a \), and effective cross section area, \( A_c \),

\[
AP_g = W_a A_c.
\]  

(3.7)

In the iterative optimization procedure of inductor design, the AP checking is implemented in each round to check the power handling capability of the core for specific peak current, peak flux density and inductance. If the calculated \( AP_e \) is equal or less than the \( AP_g \), the design parameters
are regarded as effective. Otherwise, bigger core or combining more cores in parallel should be implemented to increase the core volume, $V_{\text{core}}$, and $AP_g$ for the satisfaction of AP checking.

**Coil and air-gap design**

For the coil design of the inductor, the number of turns, $N$, combined with the air-gap, $l_g$, determines the inductance. The cross section area and the length of the coil conductor influences the copper losses. Thus, the number of turns, air-gap and cross section area are the three key factors that need to be considered in coil design [62], [63].

In an air-gaped inductor, the inductance could be derived as

$$L = \frac{4\pi N^2 A_c 10^{-4}}{l_g + (L_{MPL}/\mu_r) F_{\text{fringe}}}$$

where $L_{MPL}$, $\mu_r$ are the magnetic path length, relevant permeability and $F_{\text{fringe}}$ represents the fringing effect that can be expressed as

$$F_{\text{fringe}} = \frac{l_g}{\sqrt{A_c}} \ln\left(\frac{2W_h/l_g}{l_g}\right) + 1$$

where $W_h$ is the window height.

The total losses of the inductor, $P_{\text{total}}$, are composed of core losses, $P_{\text{core}}$, and copper losses, $P_{\text{copper}}$. And the copper losses are the sum of DC losses, $P_{\text{DC}}$, and AC losses, $P_{\text{AC}}$ [64]

$$P_{\text{total}} = P_{\text{core}} + P_{\text{copper}} = P_{\text{core}} + P_{\text{DC}} + P_{\text{AC}}.$$  \hspace{1cm} (3.10)

The core losses are calculated by the Steinmetz’s equation with frequency, $f_{sw}$, peak flux density, $B_{pk}$, and the coefficients, $a$, $b$ and $k$

$$P_{\text{core}} = k \cdot f_{sw}^a \cdot B_{pk}^b.$$  \hspace{1cm} (3.11)

The peak flux density, $B_{pk}$, is expressed with the turn number, $N$, peak inductor current, $I_{pk}$,
Figure 3.3: The distribution of (a) wire (b) PCB and (c) foil coils in E core window.

The magnetic path length, $L_{MLT}$, and permeability, $\mu_r$, result in:

$$B_{pk} = \frac{4\pi N I_{pk} 10^{-2}}{l_g + (L_{MLT}/\mu_r)}.$$  \hspace{1cm} (3.12)

The copper losses can be derived in detail as

$$P_{copper} = (I_{DC}^2 + I_{AC,\text{rms}}^2) R_{DC} RF$$ \hspace{1cm} (3.13)

where $I_{DC,\text{rms}}$ and $I_{DC,\text{rms}}$ are the DC and AC components of RMS currents. $R_{DC}$ is the DC resistance which is relevant to the mean length per turn, $L_{MLT}$, number of turns, $N$, cross section area, $A$, and resistivity, $\rho$, of the coil conductor in (3.14). $RF$ is the ratio of AC and DC resistance called resistance factor. However, the AC resistance, $R_{AC} = R_{DC} RF$, is a much more complex variable that depends on the frequency, coil structure and routing method and will be analyzed in next section.

$$R_{DC} = \frac{\rho N L_{MLT}}{A}$$ \hspace{1cm} (3.14)
Turn number and air-gap adjustment

The adjustments of turn number and air-gap mainly aim at avoiding saturation and tuning the inductance as is shown in (3.8) and (3.12). In the optimization procedure of inductor design, the number of turns are swept from the maximum allowable value to find the minimum inductor losses. In the mean time, the air-gap is adjusted accordingly to maintain a desired inductance. The maximum allowable turn number, $N_{\text{max}}$, is restricted by the window area, $W_a$, and the cross section area of the coil conductor. The derivation of $N_{\text{max}}$ is different for the wired coil and PCB coil in Fig. 3.3. For the wired coil with diameter of $d$

$$N_{\text{wire, max}} = \frac{W_w (2W_h + l_g)}{d}.$$ \hspace{1cm} (3.15)

For the PCB coil with thickness of $h$ and length of $l_{\text{PCB}}$

$$N_{\text{PCB, max}} = \frac{W_w}{l_{\text{PCB}}} \frac{(2W_h + l_g)}{h}.$$ \hspace{1cm} (3.16)

For both wired and PCB coil inductors in (3.15) and (3.16), $W_w$ and $W_h$ are the window width and height, respectively.

Iterative Searching

For the iterative searching of the inductor optimization, the number of turns is swept to find the minimum inductor losses at each operating point of desired switching frequency. Specifically,

<table>
<thead>
<tr>
<th>Table 3.1: High frequency high power inductor design parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>DC bus voltage</td>
</tr>
<tr>
<td>AC RMS current</td>
</tr>
<tr>
<td>AC current ripple</td>
</tr>
<tr>
<td>Switching frequency range</td>
</tr>
<tr>
<td>Core volume</td>
</tr>
<tr>
<td>Winding gauge</td>
</tr>
</tbody>
</table>
at each frequency point, the turn number is swept from the largest allowable value to find the optimal turn number for minimum inductor losses while checking the saturation issue of the flux density. Thus, at each frequency value, the optimal values of turn number, airgap, core/copper losses, inductance and peak flux density are derived for the following sections of structural design. The theoretical design algorithm of flow chart is shown in Fig. 3.4. The theoretical inductor optimization is calculated based on the high frequency high power critical soft switching converter with the parameters in table 3.1 where the switching frequency is swept from 100kHz to 1MHz. At each switching frequency point, the optimal turn number, airgap, inductor losses, inductance and peak flux density are derived to achieve the minimum inductor losses. The E42/21/20-3F36 from Ferroxcube is chosen as the core cell which is a kind of ferrite material. It is a medium to high frequency power material suitable for a frequency ranged from 500kHz to 1MHz. And it has low power loss density at a wide temperature range from 25 to 100 °C. The design algorithm is aimed at optimizing the inductor parameters at every specific frequency point. And the maximum frequency point (1MHz) could be chosen as the most strict condition which will be feasible to be applied to any of the lower frequency range without violating the $B_{max}$ and AP checking. Specifically, the turn number, air-gap, inductance at 1MHz could be picked as the optimal parameters to operate in the lower frequency ranges. The optimization results of inductor design parameters at 1MHz are shown in table 3.2.

Table 3.2: Theoretical inductor design results at 1MHz

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>1MHz</td>
</tr>
<tr>
<td>Turn number</td>
<td>10</td>
</tr>
<tr>
<td>Air gap</td>
<td>1.38 cm</td>
</tr>
<tr>
<td>Core loss</td>
<td>15.3 W</td>
</tr>
<tr>
<td>Copper loss</td>
<td>24.1 W</td>
</tr>
<tr>
<td>Inductance</td>
<td>4.1 μH</td>
</tr>
<tr>
<td>Peak flux density</td>
<td>0.2 T</td>
</tr>
</tbody>
</table>
3.2 Structural Optimization

The geometrical structure of the inductor is an essential part that will influence the electrical and magnetic performances. This section covers both the coil structure and core geometrical topology. Specifically, for the coil structure design, different types of coil including litz PCB, solid PCB, litz wire, solid wire are taken into account for the considerations of high frequency AC losses, space utilization. A 3D litz PCB routing method is developed for PCB application of litz wire. For the core geometrical topology design, three types of core structures, E-E, E-I and I-I cores are analyzed and compared based on the window area and air-gap for the coil space utilization. Finally, considering different merits of trade off, three optimal prototypes are derived, fabricated and validated.
3.2.1 Coil Structure Design

The high frequency AC losses are analyzed in a solid coil conductor. For the reduction of AC losses, a 3D litz PCB routing method is developed with n layers of PCB board to emulate the litz wire. The comparison of litz and solid PCB coil is derived with high resolution FEA simulation.

**High frequency AC loss analysis**

The copper losses are generated by the coil conductor which include DC losses and AC losses as is shown in (3.13). The DC, AC rms currents and DC resistance, \( I_{DC,\text{rms}} \), \( I_{AC,\text{rms}} \) and \( R_{DC} \), could be directly derived mathematically. However, the AC resistance, \( R_{AC} \), is complicate to derive theoretically, especially in the high frequency applications. The Dowell’s equation could be applied to estimate the AC resistance [53], [64], [65], [66]. To analyze the AC losses of the conductor geometrically, the traditional coil structure could be mainly divided into rectangular foil solid conductor, round wire solid conductor and round wire litz conductor. The complexity of estimating the AC resistance results from the factors of skin effect and proximity effect.

The skin effect is induced by the internal current of the conductor which generates a magnetic field that makes the current density lower in the center and higher in the surface. On the other hand, the proximity effect is induced by the adjacent conductors that produce magnetic fields and influence the current density distribution: higher in the outer wire and lower in the inner wire. Thus, both the skin and proximity effects will distort the current density distribution of the conductor and the AC resistance will be increased by the rise of frequency.

In PCB solid winding conductor, the AC resistance can be derived in (3.17) as

\[
R_{AC,\text{PCB}} = R_{\text{skin}} + R_{\text{prox}} = \frac{L_{\text{PCB}}}{2\sigma W h} \left( \frac{h}{\delta} \right) \left( \frac{\sin(h/\delta) + \sin(h/\delta)}{\cosh(h/\delta) - \cos(h/\delta)} \right) + \frac{1}{12} h w^2 \sigma B_n^2 W^3
\]

(3.17)

where \( L_{\text{PCB}} \), \( h \), \( W \), \( \delta \), \( \sigma \), \( w \), \( B_n \) are the length, thickness, width, skin depth, conductivity, angular frequency, average external magnetic field of the PCB winding.
In rectangular foil solid conductor, the AC resistance can be derived in (3.18)

\[
R_{AC,foil} = \frac{l_w m}{\delta \sigma h_w} [\zeta'_1 + \frac{2}{3} \eta_w^2 (m^2 - 1) \zeta'_2]
\]

(3.18)

where \(\zeta'_1\) is the skin effect factor

\[
\zeta'_1 = \frac{\sinh(2\Delta') + \sin(2\Delta')}{\cosh(2\Delta') - \cos(2\Delta')}
\]

(3.19)

and \(\zeta'_2\) represents the proximity effect factor

\[
\zeta'_2 = \frac{\sinh(\Delta') - \sin(\Delta')}{\cosh(\Delta') + \cos(\Delta')}.
\]

(3.20)

\(\Delta'\) is the revised penetration ratio and is expressed as

\[
\Delta' = \sqrt{\frac{h_w d_w}{h_c \delta}}.
\]

(3.21)

\(m, \delta, l_w, \sigma, h_w, h_c, d_w\) are the layer number, skin depth, layer mean length, material conductivity, layer width, core window size and foil conductor thickness, respectively.

In round wire solid conductor, the AC resistance can be derived based on the Dowell’s equation in (3.22)

\[
R_{AC,wire} = \frac{l_w m N}{\delta \sigma \sqrt{\pi/4d}} [\zeta'_1 + \frac{2}{3} \left(\frac{\sqrt{\pi/4dN}}{h_w}\right)^2 (m^2 - 1) \zeta'_2]
\]

(3.22)

where \(d, N\) are the diameter and turn number of the round wire solid coil.

The mathematical calculation for PCB, foil and round conductor AC resistance are based on the parameters in Fig. 3.3.

The AC resistance is highly relevant to the frequency of the current excitation and a higher frequency will result in a thinner skin depth, \(\delta\), which is derived by resistivity, \(\rho\), switching frequency, \(f_{sw}\), and permeability, \(\mu\)
\[ \delta = \sqrt{\frac{\rho}{f_s \pi \mu}}. \] (3.23)

This skin depth, \( \delta \), will affect the revised penetration ratio, \( \Delta' \), in (3.21) and thus influence the skin and proximity effect factors, \( \zeta_1', \zeta_2' \), in (3.19) and (3.20). Finally, the AC resistance will be increased with the rise of frequency as is shown in (3.18) for foil conductor and (3.22) for round conductor, respectively.

Due to high AC resistance of solid conductor, the AC copper losses could be increased significantly in high switching frequency power converter filtering system. The resistance factor \( RF \), defined as the ratio of AC and DC resistance, can be applied to describe the performance of copper losses for specific coil.

\[ RF = \frac{R_{AC}}{R_{DC}} \] (3.24)

According to (3.18) and (3.22), the penetration ratio, switching frequency and number of turns/layers are the dominating factors that affect the resistance factor. A typical option to eliminate the AC resistance is by replacing the round solid wire with litz wire. Litz wire is fabricated by twisting multiple stranded wires to reduce the skin and proximity effects. For the skin effect, because each strand has much smaller cross section area, the influence of skin depth turns to be negligible compared to the current conducting diameter. For the proximity effect, the evenly distributed spiral strands could counteract the magnetic fields in adjacent strands. So, the proximity effect will be largely reduced. Thus, in strand level of each bundle, both skin and proximity effects are decreased effectively with litz structure. For stacked layers or multiple turns of the coil, the bundle level skin and proximity effects could also result in extra AC losses due to the adjacent bundles of wire. Despite of the bundle level effect, the litz wire is superior than solid wire in the aspect of AC losses.

In litz winding conductor, the AC resistance can be derived as [67]
\[ R_{AC,litz} = \frac{4l_w m N \zeta}{\sqrt{2} n_s \sigma \pi d_s^2} \left[ \psi_1(\zeta) - \frac{\pi^2 n_s p_f}{24} (16m^2 - 1 + \frac{24}{\pi^2}) \psi_2(\zeta) \right] \] (3.25)

where \( m, N, l_w, n_s, d_s, \zeta \) are the layer number of the winding, turn number of litz wire per layer, number of strands per bundle and strand diameter, respectively. The variables of \( \psi_1(\zeta) \) and \( \psi_2(\zeta) \) are the skin effect and proximity effect losses which are expressed as Bessel functions and can be derived by a Taylor-series expansion [67]

\[
\psi_1(\zeta) = 2\sqrt{2}(\zeta + \frac{1}{328}\zeta^3 - \frac{1}{3214}\zeta^5 + \ldots) \] (3.26a)

\[
\psi_2(\zeta) = 0.5\sqrt{2}(-\frac{1}{25}\zeta^3 + \frac{1}{212}\zeta^7 + \ldots). \] (3.26b)

**3D litz PCB routing method for AC losses reduction**

Although litz wire could reduce the AC losses significantly, the cost and insulation restrict the litz wire from wide application because each strand of the bundle inside the litz wire needs to be insulated. On the other hand, the PCB winding has the merits of inherent insulation capability, convenience of assembly and high window space utilization. This chapter develops a 3D litz PCB routing method to combine the advantages of both litz wire and PCB winding. The method is designed by applying the litz structure of round twisted wire to PCB routing for multiple layers.

The 3D routing method is aimed at emulating the twisted litz wire by following two principles: (a) Each of the strand in the PCB board should go through all the layers evenly and spirally to counteract the adjacent magnetic field; (b) The length of each strand should be equivalent to avoid uneven magnetic field among different strands.

Thus, a routing method is implemented in Fig. 3.5 which could be extended and applied to arbitrary number of strands and layers for a better emulation of round litz wire. Specifically, starting from the top-right corner of the figure, each strand will be spirally and evenly routed.
Figure 3.5: (a) 3D litz PCB routing method, 3D view of (b) separated and (c) integrated routing example.

Through all layers of the PCB board. To achieve this goal, the litz PCB is composed of six types of routing modes: left-right, right-left, external-via-up, external-via-down, internal-via-up, internal-via-down. The left-right and right-left modes are the wires that are routing directly from side to side of certain copper layer. The external-via-up and external-via-down are the vias that are distributed on both sides of PCB edges to connect between adjacent copper layers. If more than 4 layers are designed for the PCB, the internal-via-up and internal-via-down will be added which are the vias distributed inside the PCB away from the edges to connect between adjacent copper layers.

**Litz PCB design procedure**

Based on the 3D litz PCB routing method, a specific litz PCB winding design procedure is shown in this subsection which includes the routing method, copper thickness, strand number, trace width and layer number.

Firstly, the thickness of the PCB copper layer, \( t_{PCB} \), is designed according to the skin depth equation in (3.23). To avoid the conductor being influenced by the skin effect from both top and
Figure 3.6: Four types of litz PCB routing structures with different strand number and trace width: (a) Litz PCB 4×7 Strands, 16mils trace width (b) Litz PCB 4×10 Strands, 8mils trace width (c) Litz PCB 4×2×5 Strands, 8mils trace width and (d) Litz PCB 4×16 Strands, 5mils trace width.

bottom surfaces of the PCB winding, the thickness of copper trace should be less than twice of the skin depth

\[ t_{PCB} \leq 2\delta. \]  \hspace{1cm} (3.27)

The targeted maximum switching frequency is 1MHz. Given the resistivity of copper and the targeted maximum switching frequency, the skin depth is calculated as 0.0652mm. So, the thickness of the PCB copper layer should be less than twice of the skin depth which is 0.1304mm. Because the fabrication of PCB copper thickness is measured with ounce, 3oz (0.1067mm) is the most
Figure 3.7: Comparison of resistance factor with different frequencies (a) for a single PCB with different combinations of strand number and trace width (b) for different stacked number of the desired 4x10 strand type of litz PCB and solid PCB structures.

satisfied thickness option.

Secondly, the number of strand, $N_s$, and trace width per strand, $W_s$, are the two key parameters that need to be designed. These two parameters influence the proximity effect and window space utilization. A suitable combination of strand number and trace width could result in lower resistance factor thus lower AC losses, especially, when multiple layers of PCB need to be stacked for
the coil fabrication. Theoretically, the more number of strand and the thinner trace width, the less AC resistance will be induced. However, there exist the restriction of PCB minimum trace width and window space utilization. The minimum trace width per strand is restricted by the minimum diameter of the via hole, \( d_{h,min} \). The minimum spacing between adjacent strands in the same layer is restricted by the minimum outer diameter of the via, \( d_{v,min} \). And the number of strands per layer will be defined by the core window width, \( W_w \), strand trace width, \( W_s \), and trace spacing, \( S_t \). The combination of \((N_s, W_s)\) could be designed iteratively starting from the minimum requirement of via size and window width to find the optimal resistance factor

\[
(N_s, W_s)_{optimal} = \arg\min_{(N_s, W_s)} RF(N_s, W_s, S_t)
\]

(3.28)

where \( N_s \) ranges from 0 to \( W_w/(d_{h,min} + d_{v,min}) \). The strand number could be swept with a certain step to iteratively find the optimal resistance factor with reasonably tuned values of strand width and trace spacing.

The core E42/21/20 with a window width of 9mm from Ferroxcube is taken as an example for the design of litz PCB winding. Four types of routing structures with different strand number and trace width are designed and simulated with high resolution FEA analysis in ANSYS. The PCB is set to be four layers with different combinations of (strand number, trace width) as is shown in Fig. 3.6: (4×7 Strands, 16 mils), (4×10 Strands, 8 mils), (4×2×5 Strands, 8 mils), (4×16 Strands, 5 mils). In each of the subfigure, a small length of four-layer litz PCB routing structure is shown and the current is expected to flow from left-bottom of the input terminal to the right-top of the output terminal.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>4×7</th>
<th>4×10</th>
<th>4×2×5</th>
<th>4×16</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC loss (mW) @60Hz</td>
<td>108.4</td>
<td>154.1</td>
<td>154.9</td>
<td>149.4</td>
</tr>
<tr>
<td>AC loss (mW) @500kHz</td>
<td>134.1</td>
<td>163.4</td>
<td>177.5</td>
<td>167.4</td>
</tr>
<tr>
<td>AC loss (mW) @1MHz</td>
<td>160.4</td>
<td>176.5</td>
<td>192.5</td>
<td>181</td>
</tr>
<tr>
<td>RF=Rac/Rdc (pu) @500kHz</td>
<td>1.24</td>
<td>1.06</td>
<td>1.15</td>
<td>1.12</td>
</tr>
<tr>
<td>RF=Rac/Rdc (pu) @1MHz</td>
<td>1.48</td>
<td>1.14</td>
<td>1.24</td>
<td>1.21</td>
</tr>
</tbody>
</table>
From Fig. 3.6(a) to 3.6(d), the strand number is increased from 28 to 64. Accordingly, due to the core window width limitation, the trace width per strand is reduced from 16 mils to 5 mils. Specifically, in Fig. 3.6(a), 3.6(b) and 3.6(d), the single bundle types of spirally twisted litz PCB are designed with different strand numbers. Also, in Fig. 3.6(c), 5 bundles of strands are twisted respectively and connected in parallel as a whole in which each bundle has 8 strands. The AC losses and resistance factors of the four structures are listed in Table 3.3 and Fig. 3.7(a) to analyze the skin/proximity effects on the proposed litz PCB. From the illustrated results, the (4×10 Strands, 8 mils) litz routing structure has the smallest resistance factor which is more suitable for the high frequency application especially when stacking multiple PCB boards to form a specific number of turns for inductor winding.

The via to be applied in the litz PCB winding design is hollow type with outer and inner diameters of 12mil and 6mil, respectively. The high frequency loss model of the via is also built with ANSYS to analyze the impact of via on losses. The loss per via at 500kHz, 25A current is 25.63μW. For a piece of litz winding, there are totally 54 vias including 10, 8 on the two shorter sides, 18 on both longer sides. They are connected in parallel within each side and in series among the four sides. Thus, the total losses induced by the via is 8.61μW which is 0.005% of the litz PCB AC losses and can be neglected.

**Litz PCB vs. solid PCB**

Considering the final inductor prototype, multiple turns of coil requires the litz PCB to be stacked for multiple layers. Thus the proximity effect will dominate the copper losses and the resistance factor will be increased with the stacked layer number. In this subsection, the litz PCB is compared with solid PCB coil in the aspects of copper losses and resistance factor at different frequency. Also, the number of stacked PCB layers are taken into account for the AC resistance analysis. Based on the results in Fig. 3.7(a), (4×10 Strands, 8 mils) litz routing structure is chosen as the optimal litz winding solution for the core of E42/21/20 due to the least resistance factor. Also, a solid PCB winding layer with the same 3D sizes as the litz PCB layer is selected for
comparison. To analyze the resistance factor performance of different number of stacked solid or litz PCB layers, 4, 8, 12 and 16 layers of litz and solid PCB windings are simulated with the same current excitation under different frequencies. The resistance factors of the 8 types of PCB winding cases are plotted in Fig. 3.7(b) with frequency ranged from 100 kHz to 1 MHz. The results show that the designed litz PCB winding structure has 2 to 3 times lower resistance factor than the solid PCB at the same number of stacked layers. Thus, the AC copper losses of the litz PCB is lower than the solid PCB proportionally. For the E core setup, the 3D view of the proposed 4 layer litz PCB winding and the top views of each layer are shown in Fig. 3.8 and 3.9, respectively. What is noteworthy is that the four right angle corners of the litz PCB layout are designed as solid structure because the principle of litz routing requires the length of each strand to be equivalent to avoid uneven magnetic field. The solid design of winding corners guarantees that all the traces between two solid corners have the same length despite the diagonal lines may reach the edges. Since whenever a trace reaches the edge, the via will help the trace switch the layer and go towards another symmetric diagonal direction. For the terminal of the traces in Fig. 3.8 and Fig. 3.9, solid terminal pads and castellated holes are designed to connect among PCB winding boards. These castellated holes help to mount one PCB winding board on top of another during assembly. Such holes provide proper alignment between the winding boards while soldering. Thus, the terminal pads and castellated holes contribute to the balancing of winding length for every turn.
Figure 3.9: (a) Top layer (b) second layer (c) third layer and (d) bottom layer of litz PCB design in top view.

3.2.2 Core Structure Design

This section discusses the core structure design based on the E core topology which is convenient for combined fabrication with PCB winding. A commercially available E core cell of E42/21/20 is used for the core structure design which is consistent with the theoretical design of core selection. Four types of core structures are developed based on the emphasis of different merits among the trade-offs of volume, cost and losses. The four core structures are: EE, EI, II and EA cores which have been shown in Fig. 3.10. Specifically, EE, EI, II are composed of two E cores, one E core and one I core, two I cores, respectively. The air gap of these three core structures could be adjusted by inserting different height of resin in the middle of the three legs. For the EA (E-Air) core, the airgap is not flexible and is mainly determined by the window width since the structure is
Figure 3.10: Four types of core structures: (a) EE core (b) EI core (c) II core and (d) EA core.

Core structure design based on window/airgap space and winding parallelization

The high resolution design is implemented in ANSYS for validating the proposed four core structures. For each structure, different airgap values or winding heights are simulated with different number of turns to derive the suitable inductance for critical soft switching with optimal core losses and peak flux density. Based on the soft switching requirements of inductance and current ripple in equations (3.4) and (3.5), the targeted inductance is $4\mu$H. The simulated results of the four types of cores are shown in table 3.4. In each type of the EE, EI and II core structure, different turn
numbers are constructed and swept with different airgap values to derive the optimal inductance, core losses and peak flux density. For the EA core, since the airgap is not adjustable, the total winding height is tuned for the adjustment of inductance. Specifically, table 3.4 shows the derived optimal setup parameters of four core structures and the flux density distributions after simulating different airgaps/winding heights and turn numbers for each type of the core based on the same current excitation of 50A peak-peak and frequency of 500kHz and 1MHz.

Table 3.4: Four core structures design results by sweeping the air gap or winding height and turn number

<table>
<thead>
<tr>
<th>Core type</th>
<th>EE</th>
<th>EE</th>
<th>EE</th>
<th>EI</th>
<th>EA</th>
<th>II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn number</td>
<td>10</td>
<td>6</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>Air gap (mm)</td>
<td>14</td>
<td>3</td>
<td>1</td>
<td>1.2</td>
<td>-</td>
<td>8</td>
</tr>
<tr>
<td>Winding height (mm)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>5.8</td>
<td>-</td>
</tr>
<tr>
<td>$P_{core}(W)$ @0.5MHz</td>
<td>1.9</td>
<td>4.6</td>
<td>11.6</td>
<td>7.2</td>
<td>2.7</td>
<td>0.4</td>
</tr>
<tr>
<td>$P_{core}(W)$ @1MHz</td>
<td>9.7</td>
<td>23.6</td>
<td>49.4</td>
<td>28.5</td>
<td>13.8</td>
<td>2</td>
</tr>
<tr>
<td>Inductance($\mu$H)</td>
<td>4.3</td>
<td>4.2</td>
<td>4.1</td>
<td>4.1</td>
<td>4.2</td>
<td>4.1</td>
</tr>
<tr>
<td>$B_{pk}$(T)</td>
<td>0.37</td>
<td>0.36</td>
<td>0.38</td>
<td>0.34</td>
<td>0.48</td>
<td>0.08</td>
</tr>
</tbody>
</table>
Core structure trade off analysis

The four types of core structures are designed considering different emphasis of merit trade-offs. The EE core costs more on the core material and has the largest volume. But the window height is the biggest which means more winding could be stacked in parallel to decrease the coil resistance and copper losses. II core has the smallest volume but the airgap is limited by the height of the winding coil which means the airgap needs to be no less than the coil height. Thus, the number of turns and airgap need to be carefully designed to support the desired inductance especially when considering to parallel winding coil for the reduction of copper losses. The EI core is a trade-off between the EE and II cores in the aspect of volume cost and copper losses. Lastly, for the EA core, the airgap is restricted by the open area on top of the E core. Specifically, the flux path can only go through the window width on top to finish the flux loop. Thus, the winding coil could not exceed the window upper side and the airgap is not as flexible as the other three structures. However, EA core saves half of the magnetic material which means the cost is the least. To better illustrate the flux paths of the four core structures with different airgap formations, the magnetic flux paths are shown in Fig. 3.11. The green solid arrows are the flux paths in the core and the red dotted arrows represent the flux paths in the airgap. Thus, the flexibility of adjusting airgap between EE, EI, II and EA could be seen perceptually in which the EA core has an approximately constant airgap of the window width.

For the influences of different core structures and the fringing effect on the inductor performance, three cases of inductor structure are simulated in ANSYS (under same turn number, airgap, current excitation) for validation: (1) EE core; (2) EI core with winding evenly distributed in the window; (3) EI core with winding distributed away from the airgap. The flux density and current density distributions of the three inductor cases are plotted in Fig. 3.12. The inductance, core losses are simulated as follows: case (1) Core Loss@500kHz: 4.6W, Core Loss@1MHz: 14W, L=4.4uH; case (2) Core Loss@500kHz: 4.7W, Core Loss@1MHz: 17W, L=4.6uH case (3) Core Loss@500kHz: 5.3W, Core Loss@1MHz: 19W, L=4.9uH. Thus, from the ANSYS comparison of cases (1) and (2), the EE or EI core difference does not influence too much of the inductor con-
figuration. From the ANSYS comparison of cases (2) and (3), the fringing effect caused by the distance between the winding and airgap does not have obvious effect on the inductor behavior.

Figure 3.12: Analysis of EE/EI core inductor performances with different winding distributions.

Figure 3.13: Four-layer neural network model for resistance factor of the proposed (a) litz and (b) solid PCB winding.
3.2.3 Neural Network Modeling of Litz/Solid PCB Structure

**Neural network design**

For the analytical modeling of AC losses in the litz/solid PCB winding, two 4-layer neural network models are built to analyze the resistance factors of the proposed litz/solid PCB winding under different design parameters. For the structure of the neural network, the 4-layer model consists of input layer, two hidden layers and output layer as is shown in Fig. 3.13.

Firstly, for the input layer, the key factors that could affect the resistance factor of litz PCB winding are strand number, $N_s$, trace width, $W_s$, trace thickness, $t_{PCB}$, layer number, $N_l$, and frequency, $f_{sw}$. The trace thickness could be determined by equation (3.27) to minimize the skin effect. Thus, 4 variables are configured as the input of the litz PCB neural network model including strand number, trace width, layer number and frequency. For the solid PCB winding, only trace width, layer number and frequency are needed for the input variables. Secondly, two hidden layers are designed to approximate smooth mapping for high accuracy. Different number of neurons are configured to optimize the training and testing losses. Table 3.5 shows the testing losses of the 4-layer neural network with different combinations of neuron number from 2 to 6 in the two hidden

![Figure 3.14](image-url): Training and testing losses of the (a) litz and (b) solid PCB winding neural network model.
layers where the losses are defined by Mean Squared Error (MSE) to assess the performance of the model. Based on the size of training data and input/output variables, (4, 4) and (4, 2) of neuron number combinations in the two hidden layers can achieve minimum losses of 1.2e-4 and 4.6e-4 for litz PCB and solid PCB models, respectively. Lastly, for the output layer, the resistance factor is the output of the neural network model for the analysis of litz/solid PCB winding AC losses.

The formulation of the neural network consists of the following five parts: (1) input values, \( x(k) \) (\( k=1,...,N_1 \), \( N_1=3 \) for three input variables of solid PCB model, \( N_1=4 \) for 4 input variables of litz PCB model); (2) hidden layer values, \( h_1(k) \) (hidden layer 1 neurons, \( k=1,...,N_2 \), \( k \) denotes \( k \)-th hidden layer 1 neuron), \( h_2(k) \) (hidden layer 2 neurons, \( k=1,...,N_3 \), \( k \) denotes \( k \)-th hidden layer 2 neuron); (3) output value, \( y(k) \) (\( k=1,...,N_4 \), \( k \) denotes \( k \)-th output layer neuron); (4) weight, \( W_{2mn} \) (weight from \( m \)-th input neuron to \( n \)-th hidden layer 1 neuron), \( W_{3mn} \) (weight from \( m \)-th hidden layer 1 neuron to \( n \)-th hidden layer 2 neuron), \( W_{4mn} \) (weight from \( m \)-th hidden layer 2 neuron to \( n \)-th output layer neuron); (5) bias, \( B_{2k} \) (bias of \( k \)-th hidden layer 1 neuron), \( B_{3k} \) (bias of \( k \)-th hidden layer 2 neuron), \( B_{4k} \) (bias of \( k \)-th output layer neuron).

The input values, \( x(k) \), can be imported as \([N_s; W_s; N_l; f_{sw}]\) for litz PCB model and \([W_s; N_l; f_{sw}]\) for solid PCB model.

The hidden layer values, \( h_1(k) \) and \( h_2(k) \), can be expressed as

\[
\begin{align*}
    h_1(k) &= \sum_{k=1}^{N_2} W_{2mn} x(k) + B_{2k}, m = 1, ..., N_1, n = 1, ..., N_2 \quad (3.29a) \\
    h_2(k) &= \sum_{k=1}^{N_1} W_{3mn} x(k) + B_{3k}, m = 1, ..., N_2, n = 1, ..., N_3. \quad (3.29b)
\end{align*}
\]

The output layer values, \( y(k) \), can be expressed as

\[
y(k) = \sum_{k=1}^{N_2} W_{4mn} x(k) + B_{4k}, m = 1, ..., N_3, n = 1, ..., N_4. \quad (3.30)
\]
Data training and testing

High resolution and accuracy ANSYS models for different litz PCB parameter combinations of \((N_s, W_s, N_l, f_{sw})\) and solid PCB parameter combinations of \((W_s, N_l, f_{sw})\) are imported for the training data. The Levenberg-Marquardt feed-forward backpropagation algorithm is applied for the training function to achieve a fast and accurate converging process. Fig. 3.14(a) and Fig. 3.14(b) show that the minimum testing losses of 1.2e-4 and 4.6e-4 are achieved with certain epochs of iteration for the litz PCB \((4, 4)\) and solid PCB \((4, 2)\) hidden layers neuron number combinations, respectively.

Inductor loss optimization leveraging neural network

The inductor loss optimization can be implemented leveraging the analytical neural network models of AC resistance factor for the proposed litz/solid PCB winding. The main difference between the neural network-based PCB-type inductor loss optimization and the normal inductor design process of Fig. 3.4 is that number of turns, \(n_t\), the number of paralleled PCB per turn, \(n_p\), the strand number, \(N_s\), and the trace width, \(W_s\), for litz/solid PCB winding need to be swept and optimized.

The constraints for the optimization are:

1. the multiplication of \(n_t n_p\) should be less than the maximum allowable number of stacked PCB, \(N_{max, PCB}\) (in a core window height of \(w_h\)):

   \[
n_t n_p \leq N_{max, PCB} = \frac{w_h}{t_{PCB}}.
   \]  \hspace{3cm} (3.31)

2. the multiplication of \(N_s W_s\) should be less than the core window width, \(w_w\):

   \[N_s W_s \leq w_w.\] \hspace{3cm} (3.32)

Thus, the neural network-based litz/solid PCB inductor design process can be illustrated in algorithm 1. By importing the required parameters of voltage, RMS current and ripple current,
the optimal number of turns, $n_t$, number of paralleled PCB per turn, $n_p$, strand number, $N_s$, trace width, $W_s$, and air-gap, $l_g$ for litz/solid PCB inductor can be derived with minimum power losses at desired switching frequency.

Table 3.5: Loss comparison of the four-layer neural network with different neuron number combinations in two hidden layers.

<table>
<thead>
<tr>
<th>Neuron number in (hidden layer1, hidden layer2)</th>
<th>(2, 2)</th>
<th>(2, 4)</th>
<th>(4, 2)</th>
<th>(2, 6)</th>
<th>(6, 2)</th>
<th>(4, 4)</th>
<th>(4, 6)</th>
<th>(6, 4)</th>
<th>(6, 6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Losses of litz PCB neural network model</td>
<td>1.5e-3</td>
<td>2.2e-3</td>
<td>5.2e-3</td>
<td>6.8e-3</td>
<td>7.2e-3</td>
<td>1.2e-4</td>
<td>3.9e-4</td>
<td>5.7e-4</td>
<td>6.2e-3</td>
</tr>
<tr>
<td>Losses of solid PCB neural network model</td>
<td>1.6e-2</td>
<td>7.7e-2</td>
<td>4.6e-4</td>
<td>9.1e-3</td>
<td>2.5e-2</td>
<td>2.8e-3</td>
<td>1.4e-3</td>
<td>9.9e-4</td>
<td>4.9e-3</td>
</tr>
</tbody>
</table>

Figure 3.15: (a) Litz PCB and (b) solid PCB winding prototypes.

### 3.3 Prototyping Results

The designed inductors are prototyped in this section for the loss, volume and cost comparison. Based on the theoretical and practical core/winding design, 10 prototypes of EE/El/EA/II core structures combined with litz wire/litz PCB/solid PCB windings are built for a comprehensive analysis.

#### 3.3.1 Prototype Finalization

Firstly, the litz and solid PCB windings are fabricated as is shown in Fig. 3.15. Based on the resistance factor comparison in Fig. 3.7(a), the (4×10 Strands, 8 mils) litz routing structure has
Algorithm 1 PCB Winding Inductor Design Optimization

1: Initialize the parameters for $V_{dc}$, $I_{rms}$, $\Delta i_L$;
2: for $f_{sw}=$100kHz:10kHz:1MHz do
3: calculate $L$ by (3.4) or (3.5);
4: check $AP$ by solving (3.12);
5: calculate $N_{max,PCB}$ by (3.31);
6: calculate air-gap by (3.8);
7: calculate peak flux density by (3.12);
8: check if $B_{pk} \leq B_{max}$;
9: $n_t \leftarrow 1, n_p \leftarrow 1, N_s \leftarrow 1, W_s \leftarrow 4mil$;
10: while $n_t \leq N_{max,PCB}$ do
11: while $n_t n_p \leq N_{max,PCB}$ do
12: for $N_s=1:4:80$ do
13: while $N_s W_s \leq w_w$ do
14: calculate core losses by (3.11);
15: calculate copper losses by (3.29), (3.30);
16: calculate air-gap by (3.8);
17: calculate peak flux density by (3.12);
18: check if $B_{pk} \leq B_{max}$;
19: $W_s = W_s + 4mil$;
20: end while
21: $W_s \leftarrow 4mil$;
22: end for
23: $n_p = n_p + 1$;
24: end while
25: $n_p \leftarrow 1$;
26: $n_t = n_t + 1$;
27: end while
28: find optimal $n_t, n_p, N_s, W_s, l_g$ with minimum losses;
29: end for
Figure 3.16: Resistance factor measurements of different layers of litz/solid PCB windings and round normal/litz wires with different frequencies.

Figure 3.17: Proposed inductor prototypes: (a) EE, 10 turns, litz wire (b) EE, 6 turns, litz wire (c) EE, 4 turns, litz PCB (d) EE, 4 turns, solid PCB (e) EA, 5 turns, litz PCB (f) EA, 5 turns, solid PCB (g) EI, 4 turns, litz PCB (h) EI, 4 turns, Solid PCB (i) II, 8 turns, Litz PCB (j) II, 8 turns, Solid PCB.
the smallest resistance factor and is selected as the litz PCB winding prototype. The resistance factor of the prototyped litz/solid PCB winding is measured with LCR meter by stacking different layers as is shown in Fig. 3.16. The measured RF is consistent with the ANSYS analysis in Fig. 3.7(b). Litz PCB has smaller RF than solid PCB and the advantage of RF is more remarkable with increased stacked number of layers. Also, a type of AWG 8 litz wire is applied for the litz wire winding. 10 prototypes are built and shown in Fig. 3.17. From Fig. 3.17(a) to 3.17(j), the inductor prototypes are designed as: EE core, 10 turns litz wire; EE core, 6 turns litz wire; EE core, 4 turns litz PCB; EE core, 4 turns solid PCB; EA core, 5 turns litz PCB; EA core, 5 turns solid PCB; EI core, 4 turns litz PCB; EI core, 4 turns solid PCB; II core, 8 turns litz PCB; II core, 8 turns solid PCB, respectively. The prototypes are designed and fabricated based on the parameters in table 3.1. Considering the high frequency ranged from 100kHz to 1MHz and high current ripple of 50A for critical soft switching operation, the desired inductance, turn number and air-gap are following the theoretical design and core structure design with ANSYS validation in section II and III, respectively. Because the thickness of litz wire is higher than PCB winding, litz wire is only suitable for EE core with more window height as is shown in Fig. 3.17(a) and 3.17(b). On the other hand, the PCB winding is thin enough to be flexibly fit into any of the core structure’s window area. To fully utilize the window area of the cores for reducing the winding resistance, the PCB winding are stacked 8 and 4 layers in parallel per turn in EE of Fig. 3.17(c), 3.17(d) and EI core of Fig. 3.17(g), 3.17(h), respectively. Due to the limited window area of EA and II cores, the number of stacked PCB per turn is one for the EA prototypes of Fig. 3.17(e), 3.17(f) and II prototypes of Fig. 3.17(i), 3.17(j), respectively. For the EA core, the airgap is nonadjustable and determined by the width of the window area. For the II core, the airgap is limited by the total thickness of the PCB winding. Thus, EA/II inductors are designed by sweeping turn number in ANSYS to derive the desired configurations which are shown in the following section.
3.3.2 Experimental Validation

The inductor prototypes are tested with a buck converter at fixed duty cycle of 0.5 to deliver 50A current ripple at different switching frequency ranged from 100kHz to 1MHz. The testbench is shown in Fig. 3.18 including three-phase type of switch board on the right, controller board in the middle and sensing board on the left. The switch board is composed of SiC MOSFET (C2M0025120D)×6, gate driver (CRD-001)×6, DC bus capacitors (B32774D8505K, 5μF)×9 and DC voltage sensor (RP1215D). The sensing board includes three phase capacitors (B32774D8126K000, 12μF)×9, voltage sensor (RP1215D)×3, current sensor (CKSR 25-NP)×3,

![Figure 3.18: Testbench for inductor loss measurement.](image)

Figure 3.19: (a) Inductor voltage, inductor current and output voltage and (b) the zoomed waveforms at 500kHz switching frequency, 500V input voltage and 0.5 duty cycle.
power relay (T9SV1K15-12)×3. Typical inductor voltage, inductor current and output voltage waveforms at 500kHz are shown in Fig. 3.19 with zoomed views. The PCB winding width and thickness are designed for a temperature rise of less than 40 °C under the desired current rating. The thermal behaviors of designed inductors are compared with the commercial ones in Fig. 3.20. The proposed inductors have temperature rise only up to 50-60°C which are 60-70°C lower than the commercial ones. For a solid winding, the AC resistance will be increased by a factor of more than 10 when the switching frequency is reaching 500kHz as is shown in Fig. 3.16. If the winding

![Thermal behaviors of the designed and commercial inductors at 500kHz, 50A peak current](image)

Figure 3.20: Thermal behaviors of the designed and commercial inductors at 500kHz, 50A peak current: (a) EE core, litz PCB (b) EA core, solid PCB (c) SER inductor (d) AGM inductor (e) AGP-332 inductor (f) AGP-562 inductor (g) WE-0068 inductor (h) WE-1022 inductor (i) DMT2-20 inductor.
of commercial inductors are not specially designed, the AC losses will be increased proportionally. Thus, high temperature rise will occur if no active cooling system is added.

The loss, volume and cost of the 10 proposed prototypes and two typical commercial inductors are compared in Fig. 3.21 and Fig. 3.22. Specifically, Fig. 3.21(a) shows the comparison of volume and loss at 500kHz. It can be derived that the EE core litz wire inductors have the lowest losses but higher volume. II and EA core PCB inductors have the smallest volume and higher losses. EE core PCB inductors have the medium volume and losses. The minimum losses are achieved with EE core 6 and 10 turns litz wire inductors which are 13.1W and 6.5W, respectively. The least volumes are achieved with II core 8 turns and EA core 5 turns PCB inductors which are 29.5 cm$^3$ and 32.6 cm$^3$, respectively. The commercial inductor of AGM and SER have significant losses compared with the proposed inductors despite of their small volumes. Also, the loss and cost among the inductors are compared in Fig. 3.21(b). For a mass production, the cost of the PCB winding inductor is less than the litz wire inductor and the commercial ones. The EA core inductor has the least cost since it needs only one core for fabrication. The circled points in the two figures are the desired solutions for the prototype if putting different weighing factors on the loss, volume or cost. Finally, the break down of core and copper losses for the 10 designed inductors and 2 commercial inductors are listed in Fig. 3.22 with frequencies of 100kHz, 500kHz and 1MHz. The caption of each prototype from (a) to (j) are consistent in Fig. 3.17 and Fig. 3.22. Compared with the commercial ones, the designed inductors reduced the core and copper losses significantly by a factor of 5-10.

3.3.3 Observations

The following observations are derived from the conducted research:

1. The critical soft switching power converter at high power ($\geq 11kW$) and high frequency (100kHz-1MHz) requires a large current ripple ($\geq 50A$). The commercial inductors could not handle this high ripple high frequency current due to the high power losses and temperature rise ($\geq 125^\circ C$).
Figure 3.21: Comparisons of Power losses with volume and cost among the proposed prototypes and commercial products: (a) Losses and volume comparison (b) Losses and cost comparison.

Figure 3.22: Comparison of inductor core and copper losses break down at 100kHz, 500kHz and 1MHz.

2. The conducted research provides the specially designed critical soft switching inductors to handle high frequency large current ripple working conditions by reducing the overall losses
by a factor of 5-10 and temperature rise by a factor of 2-3.

3. The AC winding losses can be reduced by introducing litz wire with large number of strand. But the cost and volume of litz wire are high due to the thick outer insulation jacket and manufacturing process.

4. Careful design of PCB litz/solid windings can be a substitute for the litz wire in the reduction of high frequency AC copper losses. On one hand, the thickness of PCB copper could be flexibly adjusted to reduce the high frequency AC losses caused by the skin effect. On the other hand, multiple pieces of PCB could be stacked in parallel per turn to fit into the core area for the reduction of the equivalent DC resistance.

5. The litz PCB 3D layout method could largely emulate the litz wire capability for attenuating the AC losses of skin and proximity effects by performing a small resistance factor.

6. The four core structures have advantages in different aspects. EE and EI core have more window area for paralleling more PCB to reduce the DC resistance. EA and II cores have less volume and cost. The flexibility of adjusting the stacked number of PCB for EE and EI cores

![Figure 3.23: Ratings of performance for four of the desired inductor prototypes.](image-url)
are better than EA and II cores.

7. For the selection of inductor among the designed prototypes, if volume and cost are the two primary considerations, II 8 turns inductor and EA 5 turns inductor can be the preferences which reduce 50% of the volume and 75% of the cost compared to EE inductors. On the other hand, if the losses are the primary considerations, EE 10 turns litz wire inductor and EE 4 turn litz PCB inductor can be the preferences which reduce 40-60% of the losses compared to the II or EA inductors. Specifically for the core structure selection, the EE core has more window area for winding and is suitable for round litz wire (high diameter) and high inductance applications (more turn number). II core window area is restricted by the air-gap. Thus it is suitable for PCB winding (low thickness) and low inductance applications (less turn number).

8. For the selection of litz or solid PCB windings, the AC resistance can be calculated to guide for selection which are based on the DC resistance of two PCB windings, \( R_{DC,litz} \) and \( R_{DC,solid} \), in Fig. 3.15, number of turns, \( n_t \), and number of paralleled PCB per turn, \( n_p \), resistance factor at a stacked PCB number of \( n_p \times n_t \), \( RF_{n_p \times n_t} \). The total AC resistance of an inductor, \( R_{AC,litz} \) or \( R_{AC,solid} \), can be expressed as

\[
R_{AC,litz} = \frac{R_{DC,litz}n_t}{n_p}RF_{litz,n_p \times n_t}, \quad (3.33)
\]

\[
R_{AC,solid} = \frac{R_{DC,solid}n_t}{n_p}RF_{solid,n_p \times n_t}, \quad (3.34)
\]

Thus, at a certain stacked PCB number of \( n_p \times n_t \) inductor prototype, if \( R_{AC,litz} \) is less than \( R_{AC,solid} \) which means litz PCB has less copper losses, litz PCB winding can be chosen as preference. On the other hand, solid PCB can be the option. Based on the calculation in (3.33) and (3.34) and data in Fig. 3.7 and 3.16, in less stacked PCB number of \( n_p \times n_t \) prototypes of EA and II core inductors, the solid PCB has less copper losses than litz PCB because the DC resistance dominates the copper losses more than the resistance factor. However, when the
total stacked number of PCB is larger than 20 layers in EE core inductor, the litz PCB will prevail due to the litz layout’s more capability than solid PCB at reducing the resistance factor at higher stacked number of PCB setups.

9. For the inductor optimization design methods that are developed in this chapter, the round wire type of litz winding inductors are designed based on the analytical litz wire AC loss equations. The PCB type of litz/solid winding inductors are designed based on the proposed neural network model for the derivation of optimal PCB winding structures.

To summarize for the prototyping designs, the desired inductor setups are labeled with red circles in Fig. 3.21(a) and Fig. 3.21(b), respectively by considering different weighing factors on loss, volume or cost. EE litz wire inductor has low losses, higher cost and volume. EE litz PCB inductor has lower volume, higher losses and lower cost. II and EA core inductors have low volume, low cost and higher losses. All the designs are based on the critical soft switching conditions of high frequency (100kHz-1MHz), high current ripple (50A) which could not be handled by the benchmarked commercial inductors due to the high loss and temperature rise. Also a performance rating comparison radar chart of five desired prototypes scored from 6 to 10 is shown in Fig. 3.23 to address the advantages of different designs in the aspects of losses, volume, cost and weight. For each comparative item, the five prototypes are ordered and scored from 6 to 10 to show their strength in a unified radar chart system.

Table 3.6: Overall Comparisons of the proposed prototypes, commercial inductors and theoretical design

<table>
<thead>
<tr>
<th></th>
<th>(a)</th>
<th>(b)</th>
<th>(c)</th>
<th>(d)</th>
<th>(e)</th>
<th>(f)</th>
<th>(g)</th>
<th>(h)</th>
<th>(i)</th>
<th>(j)</th>
<th>SER</th>
<th>AGM</th>
<th>332</th>
<th>562</th>
<th>Calculation</th>
</tr>
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<tbody>
<tr>
<td>Loss (W) @100kHz</td>
<td>0.9</td>
<td>0.5</td>
<td>4.8</td>
<td>5.5</td>
<td>8.4</td>
<td>11.7</td>
<td>14.8</td>
<td>11.6</td>
<td>11.4</td>
<td>9.8</td>
<td>17.6</td>
<td>20.6</td>
<td>10.4</td>
<td>14.7</td>
<td>6.3</td>
</tr>
<tr>
<td>Loss (W) @500kHz</td>
<td>6.2</td>
<td>6.5</td>
<td>15.3</td>
<td>15.6</td>
<td>39.9</td>
<td>28.1</td>
<td>39.6</td>
<td>28.1</td>
<td>30.5</td>
<td>21.9</td>
<td>97.2</td>
<td>42.8</td>
<td>57.5</td>
<td>81</td>
<td>19.2</td>
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<td>Loss (W) @1MHz</td>
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<td>55.6</td>
<td>56.4</td>
<td>85.6</td>
<td>77.8</td>
<td>85.7</td>
<td>65.1</td>
<td>63.7</td>
<td>29.4</td>
<td>359.4</td>
<td>137</td>
<td>212.6</td>
<td>299.5</td>
<td>39.5</td>
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<tr>
<td>Volume (cm$^3$)</td>
<td>89.3</td>
<td>71.8</td>
<td>66.8</td>
<td>66.8</td>
<td>32.6</td>
<td>32.6</td>
<td>43.5</td>
<td>43.5</td>
<td>29.5</td>
<td>29.5</td>
<td>10.7</td>
<td>12</td>
<td>44.5</td>
<td>44.5</td>
<td>75</td>
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<tr>
<td>Cost ($)</td>
<td>72</td>
<td>48</td>
<td>44.4</td>
<td>44.4</td>
<td>9</td>
<td>9</td>
<td>25.2</td>
<td>25.2</td>
<td>12.6</td>
<td>12.6</td>
<td>32</td>
<td>9.6</td>
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<td>51</td>
<td>35.7</td>
<td>135</td>
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<td>122</td>
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</table>
3.4 Summary

This chapter develops a theoretical design method for high frequency and high efficiency inductor especially for critical soft switching in high current ripple application. The optimal design parameters are derived with the minimization of inductor losses. Also, the topological design of core and coil structures are proposed. Specifically, for the coil, a 3D litz PCB routing method and designing procedures are developed to reduce the AC losses. For the core, four types of core structures, EE, EI, II, EA, are developed for different merits of trade-off including core losses, volume and cost. A neural network-based litz/solid PCB winding AC loss modeling method is developed to analytically optimize the losses of the PCB inductor design. Finally, a comprehensive analysis and comparison of the proposed designs with typical commercial inductors shows the advantages of the proposed inductors in the aspect of high frequency high ripple losses and cost. Power losses, temperature rise and cost are reduced by factors of 10, 2.5 and 3, respectively, with the proposed core and coil structures for the high frequency high current ripple critical soft switching applications.
Chapter 4: Model Predictive Control for Modular Power Converters

Model predictive control (MPC) is an advanced control technique that is gaining more attention with the increasing demand of better system dynamic performance in power electronics. Different from the conventional proportional-integral (PI) control, the MPC has a better transient performance in the aspects of rising-time, steady-state error, overshoot and disturbance rejection. Especially in high-order filtered power converter system, such as $LCL$ filtered converter, there exists an intrinsic resonance frequency that can cause oscillation or instability issues with a conventional PI controller [68]. The resonance cannot be naturally attenuated by PI control.

Passive/active damping resistors can be added in the physical/control loops to compensate for the resonance [69]. However, on one hand, a passive resistor in the main physical loop will introduce extra power losses [70]. On the other hand, the active damping method requires extra voltage/current sensors that brings more system cost [71], [72]. Besides the hardware solutions of passive/active damping methods with extra physical resistors/sensors, another option to attenuate the resonance is notch filter from the software perspective [73]. The notch filter can be added at the resonant frequency of the $LCL$ filter to compensate for the resonant spikes. However, the inserted notch filter will also reduce the control bandwidth and slow down the reference tracking. Notch filter is a desired solution to reduce the high frequency EMI noise [74]. But at the same time, the system dynamic performance might be deteriorated.

MPC is capable of increasing the control bandwidth to achieve a high reference tracking speed [75], [76]. Based on this characteristic of MPC, the resonant frequency of an $LCL$ filtered converter can be shifted to a higher range by down-sizing the filter values and increasing the switching frequency [77], [78]. With the advantageous dynamic performance of MPC, the volume and weight of $LCL$ filter can be reduced. Thus, the system cost will be saved. Another intrinsic function of MPC is active damping for $LCL$ resonance which has not been studied in detail [79]. The
MPC can be functioned as an active damping control block that compensates the system resonance especially in a cascaded PI+MPC control architecture. Thus, the stability of the system can be improved which makes it possible to enlarge the proportional gain and increase the control bandwidth without exciting oscillation [80].

This chapter designs a cascaded modular model predictive control architecture for a modified non-isolated LCL filtered grid-connected inverter. The proposed method is configured as continuous control set model predictive control (CCS-MPC) for the implementation. The designed MMPC includes an upper level grid side inductor current PI control and lower level per phase switch side inductor, output capacitor (LC) filter MPC control. The inner loop MPC can be functioned as an active damping term to attenuate the resonance and improve the system stability. Thus, the control bandwidth can be increased by enlarging the outer loop gain without exciting oscillations. Also, since only the switch side LC parameters are leveraged for the MPC state space model and the grid side inductor current is controlled by the PI, the uncertainty of grid side inductance will not influence the control performance. This chapter is organized as follows. Firstly, the modified non-isolated LCL filtered inverter is introduced with the system modeling in abc and dq0 reference frames. The modified topology is capable of bypassing the leakage current from flowing into the grid. Secondly, three control structures are designed for the modified non-isolated converter with zero-sequence stabilization capabilities to attenuate the leakage current which include PI control, PI control+notch filter, PI control cascaded with MMPC. Thirdly, three control architectures are compared and analyzed with transfer functions to study the resonance rejection capabilities. The cascaded MMPC method attenuates most of the resonance and achieves the highest control bandwidth with the help of intrinsic active damping capability. An optimal control design method is developed for the cascaded MMPC to achieve better dynamic performance. Finally, the active damping analysis and proposed control design method are validated experimentally.
Figure 4.1: Non-isolated $LCL$ inverter with low leakage current.

Figure 4.2: Equivalent $LCL$ circuit with consideration of ESR.

Figure 4.3: $LCL$ plant model with consideration of ESR.

4.1 $LCL$ System Modeling

The $LCL$ system modeling is based on a modified non-isolated three-phase DC/AC converter which has been shown in Fig. 4.1. Several methods have been proposed to improve the common mode performance of the traditional DC/AC converters. [81] connected the grid neutral to the three-phase output capacitors common point for the compensation of unbalanced three-phase power system. [82] inserted a grounding capacitor between the three-phase output capacitors common point and the ground to create a zero sequence bypassing path to reduce the leakage current. [83] introduced a fourth leg to be connected between the common point of three-phase output ca-
pacitors and DC bus neutral to attenuate the common mode voltage. [84] directly connected the fourth leg to the three-phase output capacitors common point with an extra $LC$ circuit to stabilize the common mode voltage. Most of them cost extra switches to attenuate the common mode voltage. Different from the traditional two-level three-phase DC/AC converter, the common point of three-phase capacitors is connected to the DC bus positive/negative terminals to create a by-passing path for zero-sequence capacitor voltage and zero-sequence switch side inductor current control. By leveraging the topological modification and zero-sequence control methods, the common mode voltage can be stabilized to reduce the leakage current. From the perspective of system dynamic performance, the state space equations and transfer functions of the $LCL$ plant model are derived for optimal design.

4.1.1 DC/AC $LCL$ Plant Modeling

For a precise modeling of the $LCL$ filtered converter system, the equivalent series resistors (ESR) of the switch side and grid side inductors are both taken into considerations [85], [86]. For per phase switch side inductor current, $i_{Lfs}$, capacitor voltage, $v_{Cf}$, grid side inductor current, $i_{Lfg}$, grid voltage, $v_g$ and phase leg output voltage, $v_x$, the equivalent $LCL$ circuit with ESR has been

Figure 4.4: $LCL$ plant model transfer function bode plots with consideration of ESR.
shown in Fig. 4.2. The corresponding state space equations can be expressed as:

\[
L_{fs} \frac{d i_{Lfs}}{dt} = -v_{Cf} - R_{Lfs} i_{Lfs} + v_x \quad (4.1a)
\]

\[
C_f \frac{d v_{Cf}}{dt} = i_{Lfs} - i_{Lfg} \quad (4.1b)
\]

\[
L_{fg} \frac{d i_{Lfg}}{dt} = v_{Cf} - R_{Lfg} i_{Lfg} - v_g \quad (4.1c)
\]

where \(L_{fs}, C_f\) and \(L_{fg}\) are the switch side inductor, output capacitor and grid side inductor, respectively. \(R_{Lfs}\) and \(R_{Lfg}\) are the ESR of the switch side inductor and grid side inductor, respectively.

To further derive the standardized format for transfer function, the state space equations can be expressed as matrix format [87]:

\[
\frac{dX}{dt} = AX + B_c v_x + B_g v_g \quad (4.2a)
\]

\[
i_{Lfs} = C_c X \quad (4.2b)
\]

\[
i_{Lfg} = C_g X \quad (4.2c)
\]

where \(X\) is the state variable matrix and can be illustrated as:

\[
X = \begin{bmatrix}
i_{Lfs} \\
v_{Cf} \\
i_{Lfg}
\end{bmatrix} \quad (4.3)
\]

\(A, B_c, B_g, C_c, C_g\) are the system matrices and can be expressed as:
Based on the state space matrix equations, the transfer functions can be derived accordingly to illustrate the \( LCL \) plant model. Specifically, the transfer function from phase leg output voltage, \( v_x \), to switch side inductor current, \( i_{Lfs} \), can be expressed as:

\[
G_{LCL,vx2L}(s) = \frac{i_{Lfs}(s)}{v_x(s)} = C_c(sI - A)^{-1}B_c, \tag{4.5}
\]

where \( I \) is the \( 3 \times 3 \) identity matrix. The transfer function from phase leg output voltage, \( v_x \), to grid side inductor current, \( i_{Lfg} \), can be expressed as:

\[
G_{LCL,vx2g}(s) = \frac{i_{Lfg}(s)}{v_x(s)} = C_g(sI - A)^{-1}B_c. \tag{4.6}
\]

For the illustration of the resonance issue in \( LCL \) filter system to control the grid current and consider the ESR, the equation (4.6) can be expanded as:

\[
G_{LCL,vx2Lfg}(s) = \frac{i_{Lfg}(s)}{v_x(s)} = \frac{V_{dc}}{(sL_{fs} + R_{Lfs})(sL_{fg} + R_{Lfg})sC_f + (L_{fs} + L_{fg})s + (R_{Lfs} + R_{Lfg})}. \tag{4.7}
\]
In the plant model transfer function, the quadratic term coefficient of the denominator is multiplied by the ESR of switch and grid side inductors, $R_{Lfs}$ and $R_{Lfg}$. These two ESR values are ranged at a level of milliohms which are not enough to damp the resonance because of a too small portion of quadratic term coefficient [88]. The bode plots of equations (4.5) and (4.6) has been shown in Fig. 4.4. In the resonant frequency of

$$\omega_{res} = \frac{L_{fs} + L_{fg}}{L_{fs}L_{fg}C_{f}},$$

(4.8)

there exists a convex magnitude spike which could cause system stability issue.

4.1.2 Zero-Sequence Modeling

In a traditional transformerless three-phase grid-connected inverter, a leakage current path could be excited by the high frequency fluctuation of common mode voltage [89], [90]. In a $dq0$ reference frame system, the common mode voltage is represented as the zero-sequence component. Thus, a high frequency oscillation of zero-sequence voltage can cause high leakage current in the parasitic paths [91]. The value of leakage current, $i_{lk}$, is mainly determined by the parasitic capacitance, $C_{para}$, and the change rate of zero-sequence voltage, $v_{Cf,0}$, [72]:

$$i_{lk} = C_{para} \frac{dv_{Cf,0}}{dt},$$

(4.9)

where $v_{Cf,0}$ is the mean value of three-phase output capacitor voltages, $v_{Cf,a}, v_{Cf,b}, v_{Cf,c}$. In a conventional $LCL$ filtered grid-tied inverter, the zero-sequence voltage always fluctuates in high frequency:

$$v_{Cf,0} = \frac{v_{Cf,a} + v_{Cf,b} + v_{Cf,c}}{3}.$$

(4.10)

However, with the modified non-isolated converter topology in Fig. 4.1, the zero-sequence voltage can be stabilized as half of DC bus voltage, $V_{dc}/2$. And the connections of three-phase output capacitors common points to the positive/negative DC bus terminals enables the grid side
leakage current to be bypassed and attenuated as is shown in Fig. 4.5. With the improved topology, the zero-sequence current only flows through the switch side inductors and output capacitors instead of further injecting into the grid. Leveraging the zero-sequence voltage/current control methods, the leakage current can be limited within the standard requirements of less than 30mA in an EV system by IEC 62955:2018 and IET Wiring Regulation 18th Edition (BS 7671:2018) Section 722.531.2.101 [92].

4.2 Control Structures Analysis

The control strategies of the modified LCL filtered inverter are analyzed in this section. Different from the conventional control methods of grid-connected inverters [93], the zero-sequence components of output capacitor voltage and switch side inductor current are stabilized with specific controllers. To analyze the dynamic performances and resonance behaviors of different control strategies in LCL filter system, four control structures are studied including PI control, PI control with notch filter, cascaded PI and cascaded modular model predictive control methods.
Figure 4.7: Control diagrams of the (a) PI (b) notch filtered PI (c) cascaded PI and (d) active-damping MPC for the transformerless \(LCL\) inverter.

### 4.2.1 PI Control

The PI method of control diagram is shown in Fig. 4.7(a). The grid current is transformed from \(abc\) to \(dq0\) reference frame based on Park and Clarke transformations. Then, the \(d\), \(q\) and \(0\) sequences of the grid current are controlled by PI in DC frame for a better dynamic tracking performance. \(d\), \(q\) and \(0\) are corresponding to active power, reactive power and common mode components, respectively. The output of the grid current controller will be transformed from \(dq0\) back to \(abc\) reference frame for duty cycle of PWM modulation. With the zero-sequence controller to minimize the zero-sequence grid current with a tracking reference of 0A, the common mode leakage current on the grid side can be attenuated to a low level.

The transfer functions of \(dq0\) grid current controllers can be expressed as:
\[ G_{iL_{fgd}, PI}(s) = K_p iL_{fgd} + \frac{K_i iL_{fgd}}{s} \]  
\[ G_{iL_{fgq}, PI}(s) = K_p iL_{fgq} + \frac{K_i iL_{fgq}}{s} \]  
\[ G_{iL_{f0}, PI}(s) = K_p iL_{f0} + \frac{K_i iL_{f0}}{s}. \]  

With the PI control strategy, the resonance of LCL filter in Fig. 4.4 still exists at the resonant frequency point.

### 4.2.2 PI Control with Notch Filter

To attenuate the resonance of LCL system, a notch filter can be added after the output of grid current controllers as is shown in Fig. 4.7(b). The principle of notch filter is to flatten the spike within a certain range centered at resonant frequency point. The notch filter can be designed in continuous-time as

\[ G_{Notch}(s) = \frac{s^2 + \omega_{res}^2}{s^2 + \frac{\omega_{res}}{Q}s + \omega_{res}^2} \]  

and implemented in discrete-time as difference equations. The variable \( Q \) represents the quality factor and is configured to adjust the frequency range of notch filter.

With the help of notch filter, the resonance of the peak spike from the LCL system can be attenuated. However, on one hand, another concave spike may be excited because of the notch filter. On the other hand, the added notch filter reduces the control bandwidth and slows down the dynamic performance.

### 4.2.3 Cascaded PI Control

To make a comprehensive comparison of resonance damping and dynamic performance before introducing the proposed cascaded modular model predictive control method, the cascaded PI control is analyzed as is shown in Fig. 4.7(c). The cascaded PI control diagram for the LCL filtered
inverter includes the the outer loop of grid side inductor current control and inner loop capacitor voltage control. The references for the inner loop capacitor voltage control are derived from the output of the outer loop grid side inductor current control.

The transfer functions of capacitor voltage controller can be expressed as:

\[
G_{vCf,PI}(s) = K_{p,vCf} + \frac{K_{i,vCf}}{s}
\]  

(4.13)

The output of the capacitor voltage controller will be transformed to the duty cycle for PWM modulation.

4.2.4 Cascaded Modular Model Predictive Control

To increase the control speed and solve the concave spike of PI+notch filter method and attenuate the resonance spike issue of PI control method, a cascaded modular model predictive control method is developed in this section. The control diagram of the cascaded MMPC is shown in Fig. 4.7(d). It includes two cascaded control layers: (1) the outer loop of grid side inductor current PI control in \(dq_0\) reference frame; (2) the inner loop of per phase switch side \(LC\) filter inductor current/capacitor voltage MPC control in \(abc\) reference frame and zero-sequence output capacitor voltage MPC control. The reasons for implementing the grid side inductor current PI control in \(dq_0\) and per phase switch side \(LC\) current/voltage MPC control in \(abc\) reference frames, respectively, can be concluded in two aspects: (1) the MPC has better tracking performance and transient behavior on time-varying AC reference signals than PI; (2) the outer loop grid side \(d\) and \(q\) current are corresponding to the active and reactive power, respectively. Thus, instead of configuring AC references for grid side \(abc\) phase current, \(dq\) grid current references can be directly linked to the active/reactive power control when grid services are required.

**Outer loop grid current PI control**

For the outer loop control, the grid side inductor current is firstly transformed from \(abc\) to \(dq\) reference frame with Clarke and Park transformations. Then, two PI controllers are configured to
regulate the $dq$ sequence of grid currents, $i_{Lfg,d}$ and $i_{Lfg,q}$, respectively. The $d$ and $q$ components of grid current references, $i^*_{Lfg,d}$ and $i^*_{Lfg,q}$, represent the active and reactive power, respectively. Then, the outputs of grid current controller are configured as the references for $dq$ sequence output capacitor voltages, $v^*_{Cf,d}$ and $v^*_{Cf,q}$, which will be transformed to $abc$ reference frame and configured as the references of inner loop per phase $LC$ capacitor voltage MPC.

**Zero-sequence capacitor voltage MPC**

For the stabilization of common mode voltage to bypass the grid side leakage current, the zero sequence component of output capacitor voltages is independently controlled through MPC as half of DC bus voltage. Thus, half of DC bus voltage measurement, $V_{dc}$, is configured as the reference of per phase zero sequence voltage MPC. With the zero sequence voltage MPC, the grid side leakage current can be attenuated to be lower than the standard requirement.

**Inner loop per phase $LC$ MPC**

An explicit MPC method is designed for the switch side capacitor voltage and inductor current control. As is shown in Fig. 4.7(d) of the control diagram, the three-phase capacitor voltages are controlled in $abc$ frame to follow the references from the cascaded grid current controller’s outputs. The switch side inductor currents are also regulated with the MPC by adjusting the weighing factor between $i_{Lfs,abc}$ and $u_{Cf,abc}$. The benefits to configure the MPC per phase in $abc$ frame can be concluded as: (1) the state space matrix of LC per phase is simpler than $dq$ system to implement the offline piecewise affine optimization code in a less costly DSP controller; (2) The time-varying angular speed term, $\omega$, can be omitted in the explicit MPC state space matrix for the offline optimization calculation; (3) Per phase MPC for LC is more flexible for a modular design perspective to extend the paralleled phase number and other topologies, e.g., DC/DC, single-phase DC/AC converters.

For the MPC implementation, in every control period, the MPC controller receives the measured switch side inductor current, $i_{Lfs,abc}$, output capacitor voltage, $v_{Cf,abc}$, grid side inductor
current, $i_{Lfg,abc}$, from ADC and output capacitor voltage references, $v_{Cf,abc}^*$ from the outer loop grid side inductor current PI controller. An offline generated piecewise affine search tree is applied to derive the optimal duty cycle for the explicit MPC. The state equations of switch side LC filter can be expressed as

$$i_{Lfs}(k+1) = i_{Lfs}(k) - \frac{T_s}{L_{fs}} v_{Cf}(k) + \frac{V_{dc} T_s}{L_{fs}} d(k) \quad (4.14a)$$

$$v_{Cf}(k+1) = \frac{T_s}{C_f} i_{Lfs}(k) + v_{Cf}(k) - \frac{T_s}{C_f} i_{Lfg}(k). \quad (4.14b)$$

For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the DC bus voltage during test, the last term of (4.14), $V_{dc} d(k)$, can be replaced by the phase leg output voltage, $v_x(k)$. The state-space model can be expressed in standard matrix format of

$$X_{k+1} = AX_k + Bu_k + Ee_k \quad (4.15)$$

where the variables and matrices represent

$$A = \begin{bmatrix} 1 - \frac{R_{Lfs}}{L_{fs}} & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix}, B = \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix}, E = \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix},$$

$$X_k = \begin{bmatrix} i_{Lfs}(k) \\ v_{Cf}(k) \end{bmatrix}, u_k = \begin{bmatrix} V_{dc} d(k) \end{bmatrix}, e_k = \begin{bmatrix} i_{Lfg}(k) \end{bmatrix}. \quad (4.16a)$$

In the MPC formulation, the inductor current/capacitor voltage references can be defined as $\tilde{X}$ and the tracking errors between the measurement and the references are expressed as $\tilde{X}$ which are
composed of
\[ X_k = \begin{bmatrix} i_{Lfs,ref}(k) \\ v_{Cf,ref}(k) \end{bmatrix}, \quad \tilde{X}_k = \begin{bmatrix} i_{Lfs,ref}(k) - i_{Lfs}(k) \\ v_{Cf,ref}(k) - v_{Cf}(k) \end{bmatrix}. \]  

(4.17)

Thus, the cost function includes two terms
\[
\min \sum_{k=0}^{N_c} \tilde{X}_k^T Q \tilde{X}_k + \sum_{k=0}^{N_p-1} \Delta u_k^T R \Delta u_k.
\]

(4.18)

For the penalties of the cost function, \( Q \) and \( R \) represent the weighing factor matrices that are implemented on the state values and input values, respectively.

The constraints of the MPC controller can be expressed as
\[
\tilde{X}_{k+1} = A \tilde{X}_k + Bu_k + E e_k \in \mathcal{X}
\]

(4.19)

\[
\Delta u_k = u_k - u_{k-1} \in \mathcal{U}
\]

(4.20)

\[
\begin{bmatrix} -I_{Lfs,max} \\ 0 \end{bmatrix} \leq X_k \leq \begin{bmatrix} I_{Lfs,max} \\ V_{dc} \end{bmatrix}
\]

(4.21)

\[
\begin{bmatrix} 0 \\ 0 \end{bmatrix} \leq u_k \leq \begin{bmatrix} V_{dc} \end{bmatrix}
\]

(4.22)

\[
\begin{bmatrix} -I_{Lfg,max} \end{bmatrix} \leq e_k \leq \begin{bmatrix} I_{Lfg,max} \end{bmatrix}
\]

(4.23)

For the implementation of MPC algorithm in every control period [43], the cost function in (4.18) will be solved to predict the future steps of optimal input variable, \( u_k \). And the first step of the input value will be implemented as the MPC output for the PWM modulation. Different from the PI control process, the MPC algorithm derives the optimal duty cycle by processing the state variable, \( X_k \), and tracking error, \( \tilde{X}_k \), in a linear way with specific coefficients. Since no integration procedure is needed in MPC, the dynamic performance of MPC is better than PI with less overshoot and higher tracking speed. Also, the inner loop MPC has higher control bandwidth which can be functioned as an active damping term to solve the LCL resonance. Due to the active damping and
high bandwidth of the inner loop MPC, the outer loop PI gains can be largely increased to speed up the dynamic reference tracking performance without causing extra resonance issue.

For the cascaded model predictive control of \( LCL \) filter system, a state estimator is designed to reduce the sensor count. One of the three variables, \( i_{Lfs}, v_{Cf}, i_{Lfg} \), can be estimated by the other two. The merits of the estimator include the anti-noise capability for better control performance and the reduction of sensor cost.

Specifically, the Luenberger observer can be designed to estimate the switch side inductor current, \( \hat{i}_{Lfs} \), capacitor voltage, \( \hat{v}_{Cf} \), and grid side inductor current, \( \hat{i}_{Lfg} \), with the samplings of capacitor voltage, \( v_{Cf} \), and grid side inductor current, \( i_{Lfg} \). The detailed implementation of the state estimator is introduced in Chapter 6 of the grid-tied inverter design case.

### 4.3 Optimal Control Design for Resonance Damping and Dynamic Performance

The optimal control design for resonance damping and dynamic performance of \( LCL \) filtered grid-connected inverter is analyzed in this section. Four control strategies in Fig. 4.7 are compared with transfer functions, bode plots, step responses and root locus to illustrate the active damping and dynamic performance improvement capabilities of the cascaded MMPC method [94].

#### 4.3.1 Control Plant Model Analysis

The integrated plant models of the three control strategies including \( LCL \) filter and control blocks are derived in Fig. 4.8. The former stages are the three types of control blocks with the input variable of grid side inductor current and output variable of duty cycle. The latter stage is the \( LCL \) filter plant model which has been derived in Fig. 4.3. Thus, the complete transfer functions can be expressed based on different control strategies.

**PI control transfer function**

For the first control strategy of PI method in Fig. 4.7(a), the corresponding system plant model has been shown in Fig. 4.8(a). Based on the derivations in (4.7) and (4.11), the transfer func-
Figure 4.8: Plant models of the (a) PI (b) notch filtered PI (c) cascaded PI and (d) active-damping MPC for the transformerless LCL inverter.
Figure 4.9: Typical LQR control diagram with delay compensation.

![LQR Control Diagram]

Figure 4.10: Comparison of bode plots for three control strategies (a) from $i_{Lfg, err}$ to $i_{Lfg}$ and (b) from $i_{Lfg, err}$ to $v_{Cf}$.

The transfer function from tracking error, $i_{Lfg, err}$, to the measurement, $i_{Lfg}$, of grid side inductor current can be expressed as:

$$G_{iLfg, err, PI}(s) = G_{iLfg, PI}(s) \cdot G_{LCL, vC2iLfg}(s).$$  \hspace{1cm} (4.24)

Notch filtered PI control transfer function

For the second control strategy of adding a notch filter after the PI controller to attenuate the resonance spike in Fig. 4.7(b), the corresponding system plant model has been shown in Fig.
Figure 4.11: Bode plots for cascaded PI control from (a) $i_{Lfg, err}$ to $i_{Lfg}$ and (b) $i_{Lfg, err}$ to $v_{Cf}$ with the inner loop $K_{p,v_{Cf}}$ gain swept from 1 to 625.

4.8(b). Based on the derivation of notch filter design in (4.12), the transfer function from tracking error, $i_{Lfg, err}$, to the measurement, $i_{Lfg}$, of grid side inductor current can be expressed as:

$$G_{iLfg, err2iLg,NotchPI}(s) = G_{iLfg, PI}(s) \cdot G_{Notch}(s) \cdot G_{LCL,vx2iLfg}(s).$$  \hspace{1cm} (4.25)

**Cascaded PI control transfer function**

For the third control strategy of cascaded PI controller in Fig. 4.7(c), the corresponding system plant model has been shown in Fig. 4.8(c). Based on the derivations in (4.7) and (4.13), the transfer function from tracking error of output capacitor voltage, $v_{Cf, err}$, to the measurement of grid side inductor current, $i_{Lfg}$, can be derived as:

$$G_{vCferr2iLfg,CascadedPI}(s) = G_{vCf, PI}(s) \cdot G_{LCL,vx2iLfg}(s).$$  \hspace{1cm} (4.26)

Then, the transfer function from the reference of output capacitor voltage, $v_{Cf, ref}$, to the measurement of grid side inductor current, $i_{Lfg}$, can be expressed as:
Furthermore, adding the outer loop grid side inductor current PI control, the transfer function

$$G_{\text{vCferr2iLg,CascadedPI}}(s) = \frac{G_{\text{vCferr2iLg,CascadedPI}}(s)}{1 + G_{\text{vCferr2iLg,CascadedPI}}(s)}.$$  

(4.27)
Figure 4.13: The bode plots of the PI control, notch filtered PI control and cascaded MMPC methods transfer functions from $i_{L_f g, err}$ to $i_{L_f g}$ with the cascaded MMPC (a) weighing factor Q/R swept from 100 to 800 at the $K_p$ gain of 10 and (b) $K_p$ gain swept from 10 to 40 at the Q/R of 400.

Figure 4.14: The step responses of the cascaded MMPC close loop transfer function from $i_{L_f g, err}$ to $i_{L_f g}$ with (a) weighing factor Q/R swept from 100 to 800 and (b) $K_p$ gain swept from 10 to 40.

from the tracking error, $i_{L_f g, err}$, to the measurement, $i_{L_f g}$, of grid side inductor current can be expressed as:

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Figure 4.15: The zeros and poles plots of the cascaded MMPC from $i_{Lfg,err}$ to $i_{Lfg}$ with (a) weighing factor Q/R swept from 100 to 800 and (b) $K_p$ gain swept from 10 to 40.

\[
G_{iLfgerr2iLfg,CascadedPI}(s) = G_{vCref2iLfg,CascadedPI}(s) \cdot G_{vCref2iLfg,CascadedPI}(s).
\]  
(4.28)

Then, the transfer function from the reference, $i_{Lfg,ref}$, to the measurement, $i_{Lfg}$, of grid side inductor current can be derived as:

\[
G_{iLfgref2iLfg,CascadedPI}(s) = \frac{G_{iLfgerr2iLfg,CascadedPI}(s)}{1 + G_{iLfgerr2iLfg,CascadedPI}(s)}.
\]  
(4.29)

And, based on equation (4.29) and the LCL plant model in Fig. 4.3, the transfer function from the reference of switch side inductor current, $i_{Lfg,ref}$, to the measurement of output capacitor voltage, $v_{Cf}$, can be derived as

\[
G_{iLfgref2vCf,CascadedPI}(s) = G_{iLfgref2iLfg,CascadedPI}(s) \cdot (sL_{fg} + R_{Lfg}).
\]  
(4.30)
Cascaded MMPC control transfer function

For the fourth control strategy of cascaded MMPC in Fig. 4.7(d), the corresponding system plant model has been shown in Fig. 4.8(d). The inner loop per phase switch side LC MMPC is cascaded with the outer loop of grid side inductor current control. A linear-quadratic regulator (LQR) can be applied to derive the transfer function for the MPC algorithm part in the control plant model of Fig. 4.8(d) to solve the cost function of (4.18).

A typical LQR control diagram integrated with a dynamic system is shown in Fig. 4.9 where $x, y, u, r$ represent the state variable, $[i_{Lfs}; v_{Cf}]$, output variable, $i_{Lfs}$, input variable of duty cycle, $d$, and tracking reference, $i_{Lfs,ref}$, respectively. The middle block of Fig. 4.9 is the core algorithm of MPC to calculate the optimal duty cycle which is a linear coefficient matrix, $-K$. And the MPC equation to calculate the optimal duty cycle based on the tracking error and state variable can be expressed as:

$$
d = -K \begin{bmatrix}
i_{Lfs} \\
v_{Cf} \\
v_{Cf, err}
\end{bmatrix} = -[K_{11}, K_{12}, K_{13}] \begin{bmatrix}
i_{Lfs} \\
v_{Cf} \\
v_{Cf, err}
\end{bmatrix} \tag{4.31}
$$

where $v_{Cf, err}$ is the tracking error of the MPC calculated as $v_{Cf, ref} - v_{Cf}$.

Thus, the inner loop of MPC can be expressed in the transfer function as Fig. 4.8(d). The transfer function from tracking error, $v_{Cf, err}$, to the measurement, $v_{Cf}$, of output capacitor voltage can be expressed as:

$$G_{v_{Cf, err}v_{Cf, MPC}}(s) = \frac{-K_{13}G_{LCL,vx2ig}(s)(sL_{fg} + R_{Lfg})(sL_{fs} + R_{Lfs})/V_{dc}}{(sL_{fs} + R_{Lfs}) + K_{11}[V_{dc} - G_{LCL,vx2ig}(s)(sL_{fg} + R_{Lfg})]/V_{dc} + \{(sL_{fg} + R_{Lfg}) + K_{11}[V_{dc} - G_{LCL,vx2ig}(s)(sL_{fg} + R_{Lfg})]/V_{dc} +}

K_{12}G_{LCL,vx2ig}(s)(sL_{fs} + R_{Lfs})(sL_{fg} + R_{Lfg})/V_{dc} -

K_{13}G_{LCL,vx2ig}(s)(sL_{fs} + R_{Lfs})(sL_{fg} + R_{Lfg})/V_{dc} \}}. \tag{4.32}
$$

Furthermore, the transfer function from the reference, $v_{Cf, ref}$, to the measurement, $v_{Cf}$, of
output capacitor voltage can be expressed as:

\[ G_{vC_{ref}2vC_f,MPC}(s) = \frac{G_{vC_{ferr}2vC_f,MPC}(s)}{[1 + G_{vC_{ferr}}vC_{f,MPC}(s)]}. \] (4.33)

Based on equation (4.33) and the \(LCL\) plant model in Fig. 4.3, the transfer function from the reference of output capacitor voltage, \(v_{C_{f,ref}}\), to the measurement of grid side inductor current, \(i_{L_{fg}}\), can be derived as:

\[ G_{vC_{ref}2i_{L_{fg}},MPC}(s) = \frac{G_{vC_{ferr}2vC_f,MPC}(s)}{(sL_{fg} + R_{L_{fg}})}. \] (4.34)

Then, taking the outer loop grid side inductor current PI control into consideration, the cascaded MMPC transfer function from tracking error, \(i_{L_{fg,err}}\), to the measurement, \(i_{L_{fg}}\), of grid side inductor current can be expressed as:

\[ G_{i_{L_{fg}err}2i_{L_{fg}},MPC}(s) = G_{vC_{ref}2i_{L_{fg}},MPC}(s) \cdot G_{iL_{fg,PI}}(s). \] (4.35)

The cascaded MMPC transfer function from tracking error of grid side inductor, \(i_{L_{fg,err}}\), to the measurement of output capacitor voltage, \(v_{C_f}\), can be expressed as:

\[ G_{iL_{fg}err2vC_f,MPC}(s) = G_{vC_{ref}2vC_f,MPC}(s) \cdot G_{iL_{fg,PI}}(s). \] (4.36)

4.3.2 Mechanism of Inner-loop MMPC for Active Damping

The resonance behavior and dynamic performance of the four control strategies for \(LCL\) filtered grid-connected inverter are analyzed based on the derived transfer functions. Fig. 4.10(a), 4.11(a) and Fig. 4.10(b), 4.11(b) show the bode plots comparison of transfer functions from the tracking error to the measurement of grid side inductor current and from the tracking error of grid side inductor current to the measurement of output capacitor voltage, respectively. The magnitude plots manifest that the PI control in Fig. 4.8(a) has a convex spike at the resonant frequency point. The notch filtered PI control in Fig. 4.8(b) has a concave spike at the resonant frequency point.
The cascaded PI control in Fig. 4.8(c) has a narrow bandwidth at high frequency range. The cascaded MMPC in Fig. 4.8(d) attenuates the spike at the resonant frequency point and the control bandwidth is wider than the conventional PI, notch filtered PI and cascaded PI methods.

Thus, the inner loop MPC of the cascaded MMPC is functioned as an active damping term to mitigate the resonance in \( LCL \) system. This active damping term contributes to the improvement of stability and control bandwidth. Furthermore, the fast response and active damping characteristics of the inner loop MPC permits a wider control bandwidth for the outer loop PI control. Instead of concerning about instability of resonance in the PI control method of Fig. 4.8(a), the gains of the outer loop grid side inductor PI controller can be largely increased to improve the dynamic performance. So, by carefully designing the outer loop PI control gain, \( K_p \), and the inner loop MPC weighing factor of the cascaded MMPC, \( WF = Q/R \), the \( LCL \) system dynamic performance can be further improved.

4.3.3  Cascaded Control Design for Dynamic Performance

The control design of the proposed cascaded MMPC is analyzed in this section. Two key parameters of outer loop PI control gain, \( K_p \), and the inner loop MPC weighing factor, \( WF \), need to be designed. The bode plots of open loop transfer functions, closed loop step responses and zero-pole maps are evaluated for the design procedure.

The optimal cascaded control design flowchart is shown in Fig. 4.12 which includes inner loop MPC weighing factor, \( WF \), design and outer loop grid side inductor current PI gain, \( K_p \), design. Since the inner loop MPC can attenuate the resonance spike by functioning as an active damping term, the outer loop PI gain is permitted with a larger tuning range without losing stability. The control parameter design starts from the inner loop.

Firstly, the design parameters should be initialized based on the bandwidths of inner and outer loop controllers. Typically, the PI control bandwidth, \( BW_{PI} \), is configured to be 5-10 times slower than the inner loop MPC bandwidth, \( BW_{MPC} \) [95]:

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\[ 5BW_{PI} \leq BW_{MPC} \leq 10BW_{PI}. \quad (4.37) \]

And the PI control cutoff frequency, \( \omega_c \), should be set below 30% of the LCL resonant frequency, \( \omega_{res} \):

\[ \omega_c \leq 30\% \omega_{res}. \quad (4.38) \]

The initial values for optimal PI gains design flow chart can follow the equations below [79]:

\[ K_{p,IL_{fg}} = \frac{(L_{fs} + L_{fg})f_{sw}}{3} \quad (4.39a) \]

\[ \tau_{i,IL_{fg}} = \frac{L_{fs} + L_{fg}}{R_{fs} + R_{fg}} \quad (4.39b) \]

where \( f_{sw} \) and \( \tau_{i,IL_{fg}} \) are the switching frequency and integral time constant, respectively. The initial value for weighing factor can start from a typical range of 800-1000.

Secondly, based on the initial \( WF \) and \( K_p \), the inner loop weighing factor is swept from 100 to 800. During the sweeping period, the bode plots of open loop transfer functions from \( i_{L_{fg, err}} \) to \( i_{L_{fg}} \) are derived in Fig. 4.13(a). Also, the step responses and zero-pole map of closed loop transfer functions from \( i_{L_{fg, err}} \) to \( i_{L_{fg}} \) are derived in Fig. 4.14(a) and Fig. 4.15(a), respectively. With the reduction of weighing factor, the control bandwidth is increased in Fig. 4.13(a). And the response time is decreased with more overshoot in the transient period as is shown in Fig. 4.14(a). The sweeping check conditions of inner loop MPC weighing factor are the overshoot percentage, response time and poles magnitude. Since the outer loop \( K_p \) gain is kept in low level and has not been tuned yet, the overshoot is not a big issue in the sweeping process of inner loop weighing factor. And the response time is largely determined by the outer loop \( K_p \) gain and has not been shortened yet in the inner loop sweeping process. Thus, for the sweeping procedure of weighing factor, the overshoot check condition threshold can be configured smaller than the outer
loop sweeping process. And the response time check condition threshold can be configured larger
than the outer loop sweeping process. If the overshoot is larger than 5%, response time is smaller
than 5ms or poles are outside of the unit circle, the weighing factor sweeping is stopped to entering
the outer loop PI gain sweeping procedure.

Thirdly, the outer loop PI gain is swept from 10 to 40. During the sweeping period, the bode
plots of open loop transfer functions from $i_{Lfg, err}$ to $i_{Lfg}$ are also derived in Fig. 4.13(b). Also,
the step responses and zero-pole map of closed loop transfer functions from $i_{Lfg, err}$ to $i_{Lfg}$ are
derived in Fig. 4.14(b) and Fig. 4.15(b), respectively. With the increment of gain, the control
bandwidth is increased in Fig. 4.13(b). And the response time is decreased with more overshoot
in the transient period as is shown in Fig. 4.14(b). Same sweeping check items of outer loop PI
gain are configured as the overshoot percentage, response time and poles magnitude with different
thresholds. Compared with the inner loop weighing factor sweeping, the outer loop gain sweeping
procedure addresses more on the tracking speed and less on overshoot issue, since the inner loop
MPC has been proved to guarantee an active damping function for the whole $LCL$ system stability
to attenuate the resonance. If the overshoot is larger than 10%, response time is smaller than 1ms
or poles are outside of the unit circle, the weighing factor sweeping is stopped to finalize the outer
loop PI gain sweeping procedure.

<table>
<thead>
<tr>
<th>Table 4.1: System Parameter Configurations</th>
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<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Grid voltage, $V_{grid,L-N}$</td>
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<tr>
<td>DC voltage, $V_{dc}$</td>
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<tr>
<td>Switching frequency</td>
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<tr>
<td>Switch side inductor, $L_{fs}$</td>
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<tr>
<td>Grid side inductor, $L_{fg}$</td>
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<tr>
<td>Output Capacitor, $C_f$</td>
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<tr>
<td>MOSFET</td>
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<tr>
<td>Controller</td>
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<tr>
<td>Leakage current</td>
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</tbody>
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Figure 4.16: Comparison of the experimentally captured estimation and measurement of (a) switch side inductor current (b) output capacitor voltage and (c) grid side inductor current.

Figure 4.17: Steady state waveforms of switch side inductor current, output capacitor voltage, grid side inductor current and DC bus voltage.

| Table 4.2: Control Parameters of Different Methods |
|-----------------|-----------------|
| Q/R             | $K_p$           |
| PI              | n/a             | 2, 20          |
| Notch filtered PI | n/a         | 20             |
| MMPC            | 400             | 10, 20, 30, 40 |
Figure 4.18: Steady state waveforms of three-phase grid voltage, leakage current, DC bus voltage and zero-sequence grid voltage.

Figure 4.19: (a) Transient and (b) zoomed transient waveforms of switch side inductor current, output capacitor voltage, grid side inductor current and DC bus voltage with $i_{L_{fg,q}}$ from 3A to 10A.

Figure 4.20: Cascaded MMPC transient captured ADC readings of grid side inductor current $q$ component (a) from 2A to 8A and (b) from 8A to 2A with $K_p$ gain of 10, 20, 30 and 40.
4.4 Results

The proposed optimal control design method for resonance damping and dynamic performance improvement is validated experimentally on the modified non-isolated three-phase converter with grid simulator. The testing parameters are $400-450\,V_{dc}$ to $110-120\,V_{L-N}$ with switching frequency of 80kHz. The $LCL$ filter parameters are $45\,\mu H$ for $L_f$, $12\,\mu F$ for $C_f$ and $450\,\mu H$ for...
Figure 4.23: Waveforms comparison of inductor current, output capacitor voltage, grid current and DC bus voltage for (a) PI control with $K_p$ of 20 (b) notch filtered PI control with $K_p$ of 20 (c) PI control with $K_p$ of 2 (d) MMPC control with $K_p$ of 20 and (e) cascaded PI control with $K_p$ of 2.

$L_{fg}$. C3M0021120K SiC from Cree and TMS320F28379D from TI are applied for switches and controller, respectively.
4.4.1 State Estimation Test

The state estimator combined with the MPC has been tested experimentally for the reduction of sensor count. Fig. 4.16(a), 4.16(b) and 4.16(c) show the captured ADC readings of estimation and measurement for switch side inductor current, output capacitor voltage and grid side inductor current, respectively. The switch side inductor current can be accurately estimated for MPC control purpose based on the measurement of output capacitor voltage and grid side inductor current.

4.4.2 Steady State Common Mode Test

The steady state performance of the cascaded MMPC is tested experimentally to show the stabilized zero-sequence grid voltage and reduced leakage current. Fig. 4.17 shows the switch side inductor current, output capacitor voltage, grid side inductor current and DC bus voltage in steady state. The leakage current and zero-sequence grid voltage performances are shown in Fig. 4.18 with 450V DC bus. It can be seen from the bottom waveform that the zero-sequence grid voltage has been stabilized to be constant at half of DC bus, 225V. And the leakage current has been attenuated to be less than 15mA. Thus, the developed zero-sequence voltage MPC method is capable of reducing leakage current in the modified non-isolated $LCL$ inverter. The standard requirements of leakage current in IEC and IET are also satisfied.

4.4.3 Dynamic and Stability Performance Test

The dynamic performance of the developed optimal control design method for cascaded MMPC is validated with step transient testing. Fig. 4.19 shows the transient waveforms of switch side inductor current, output capacitor voltage, grid side inductor current and DC bus voltage with a current step of 7A. The transient performance of control methods are evaluated by capturing the experimental ADC readings with current steps. Fig. 4.20(a) and Fig. 4.20(b) show the $i_{L,f,g,q}$ steps from 2A to 8A and 8A to 2A with different outer loop grid side inductor current control gains of 10, 20, 30 and 40, respectively. Thus, the optimal gain is selected as 20 based on the control parameter design flow chart. For the dynamic performance comparison of PI control, notch filtered
PI control, cascaded MMPC and cascaded PI methods, Fig. 4.21 and Fig. 4.22 show the $i_{Lfg,q}$ steps and zoomed waveforms from 2A to 8A and 8A to 2A under five testing cases: (1) PI control with $K_p$ gain of 20; (2) notch filtered PI control with $K_p$ gain of 20; (3) PI control with $K_p$ gain of 2; (4) MMPC control with $K_p$ gain of 20; (5) cascaded PI control with $K_p$ gain of 2. It can be seen that the MMPC behaves more stable than either PI control or notch filtered PI control at high $K_p$ gain of 20 with less overshoot and oscillation. Even though the PI and cascaded PI methods can act stably with a smaller $K_p$ gain of 2, the response time is much longer than MMPC. For a more intuitive comparison, the inductor current, output capacitor voltage, grid current and DC bus voltage waveforms of these five testing cases are shown in Fig. 4.23(a), 4.23(b), 4.23(c), 4.23(d) and 4.23(e), respectively. The PI control has more oscillation than MMPC method at the same high $K_p$ gain condition of 20. Even with the notch filter, a high $K_p$ gain of 20 could also oscillate the waveforms with slightly less ripple than pure PI. The cascaded PI has more oscillation than PI at a low $K_p$ of 2. The cascaded PI will diverge faster than PI method at higher $K_p$ gain. The MMPC can operate at a $K_p$ of 20 without oscillation and shorten the response time without the need of reducing the $K_p$ gain as pure PI method. Thus, the experimental comparison of PI, notch filtered PI, MMPC and cascaded PI verifies that the optimal control design method for cascaded MMPC improves the dynamic performance with shorter response time, less overshoot and less oscillation. Based on the theoretical analysis in this chapter, the improvements of MMPC is resulted from the inner loop MPC which has the function of active damping and attenuation of resonance in $LCL$ filtered grid-connected inverter. The corresponding control parameters for the experiments have been summarized in table 4.2.

4.4.4 Comparison with the State of Art

The proposed active damping MMPC is compared with the state of art for the grid-connected $LCL$ inverter MPC control methods in this section. [96] proposed an observations-based FCS-MPC method with grid side inductor current sensors for balanced and unbalanced grid voltage conditions. [97] proposed two implementations of FCS-MPC methods to eliminate the low-order
grid current harmonics and decrease the sensitivity to grid voltage distortion. [98] and [99] proposed also FCS-MPC methods to deal with the dynamic performance of grid-connected $LCL$ inverter in $\alpha\beta$ reference frame. The advantages of the proposed MMPC can be concluded in three aspects: (1) The computation burden is low to be implemented explicitly on a low cost DSP instead of the expensive FPGA for the above mentioned references. The proposed MMPC is implemented in per phase switch side $LC$ of $abc$ reference frame instead of $dq$ or $\alpha\beta$. Thus, the variable of grid angular speed is not required in the state space matrix and the order of the per phase $LC$ state space matrix is lower. The execution time for MMPC is within $4\mu s$ at each control interrupt. (2) The proposed MMPC is combined with the modified inverter topology to stabilized the zero-sequence voltage and attenuate the leakage current. This function enables the non-isolated converter applications to satisfy the grid-connection standard requirements for common mode behavior. (3) The size of offline generated piecewise affine function C code file is small to be fit into the DSP controller. Since the MMPC is implemented for per phase $LC$ in $abc$ reference frame, the explicit solver function is largely simplified and the C file is within 5KB. This size could be easily fit into the DSP memory.

4.5 Summary

This chapter develops an optimal control design method for resonance damping and dynamic performance improvement of cascaded modular model predictive control for a modified grid-connected $LCL$ inverter. The $LCL$ system is modeled to show the intrinsic resonance issue. Also, the common mode circuit is analyzed for the modified non-isolated grid-connected inverter to manifest the leakage current bypassing and zero-sequence voltage stabilization functions. Three control strategies, including PI control, notch filtered PI control and cascaded MMPC, are studied with zero-sequence stabilization capabilities to explore the dynamic and stability performance. The cascaded MMPC is validated to have the active damping function by inserting an inner loop MPC cascaded with outer loop PI control. This cascaded control structure is capable of damping the resonance and increasing the control bandwidth to improve the system dynamic performance. A
control parameter design method is finally proposed for the cascaded MMPC to derive the optimal weighing factor and gain. The experiments have validated the proposed method.
Chapter 5: Hierarchical Software-Defined Control Architecture with
MPC-Based Power Module

In practice, high performance power conversion systems require specialized design to satisfy the demands from various loads or sources. Based on the features of different interfaced applications, the corresponding power control algorithms, parametric modeling and operating robustness design might be varying. Also, the hardware circuitry topologies need specific design procedures. The repetitive power electronics design routines increase the cost both from software algorithm and hardware circuit perspectives. Firstly, an option to provide more generalized power electronics design is to introduce the modular concept. For the power conversion system with various possible interfaced applications, the basic power module can be designed to formulate different converters to meet the various demands. However, the existing modular power electronics either focus on micro-grid system level to redistribute the energy among different interfaced power sources or hardware device level to reconstruct different circuits within a certain application case [100, 101, 102]. Thus, the specific converter design is necessary for each of the application. Secondly, to manipulate the power modules, multi-layer control is typically applied for the digital control system. Similarly, the commonly used multi-layer control techniques are concentrating on either the whole micro-grid system level to manage among the distributed energy resources (DER) or individual converter level with cascaded power control methods [103, 104, 105, 106, 107, 108]. Thirdly, the generalized power module needs a robust and stable control technique to satisfy different application requirements. Conventional PI method is simple to implement. But the dynamic performance and resonant oscillation could cause operating issues under various types of energy interfaces. MPC is an advanced control technique which has better dynamic performance and higher robustness [75, 76, 77, 78, 43, 109].
This chapter proposes a hierarchical software-defined control architecture with MPC-based power modules to improve the performance of energy conversion system with reconfigurability for different applications including single/three-phase grid, motor, battery, etc. Firstly, the control architecture is introduced with the system modeling of local MPC-based power module and three types of interfaced applications. Secondly, the three-layer hierarchical control architecture is illustrated in details including central control layer, local module control layer and application layer. Thirdly, the merits of the developed control architecture are summarized with the corresponding experimental validations.
5.1 System Modeling

The proposed hierarchical control architecture is shown in Fig. 5.1. The architecture is composed of three layers which make the system reconfigurable for different types of load/source and power converter topologies. From top to bottom of Fig. 5.1, the multi-layer control architecture is constituted by central control layer, local module control layer and application layer. Specifically, the central control layer includes software-defined functions that are responsible for the recognition of different types of interfaced load/source, reconstruction of power converter, high level current/voltage/power control and generate references for local power module control. The local module control layer is composed of desired number of MPC-based power module unit as is shown in Fig. 5.2. The local power module is configured with MPC to improve the dynamic performance and attenuate the common-mode noise. The application layer defines the interface with different types of load/source including single/three-phase grid, battery, motor, etc. This section analyzes the system modeling of the key basic component (local power module) and the correspondingly formulated different applications of the proposed hierarchical control architecture.

5.1.1 Local Power Module Modeling

As is shown in Fig. 5.2, the local power module consists of the upper/lower switches, switch side inductor, upper/lower output capacitors and the high-resolution MPC controller for the per module $LC$ control. The differential equations for the local power module $LC$ filter can be ex-
pressed as:

\[
i_{Lfs}(t) = -\frac{1}{L_{fs}}u_{Cf}(t) + \frac{v_{dc}}{L_{fs}}d(t) \quad (5.1a)
\]

\[
\dot{u}_{Cf}(t) = \frac{1}{C_f}i_{Lf}(t) - \frac{1}{C_f}i_{Lfo}(t). \quad (5.1b)
\]

where \(L_{fs}\) and \(C_f\) are the switch side inductor and capacitor, respectively. \(i_{Lfs}\), \(v_{Cf}\) and \(i_{Lfo}\) are the switch side inductor current, capacitor voltage and output side current. The local MPC control algorithm is designed based on the per phase \(LC\) filter to track the reference commands from the central control layer.

5.1.2 Application Modeling

With the recognition and reconstruction of different types of load/source interfaces from the central control layer, different number of local power modules are connected with the corresponding system models to perform the specific power control algorithms. The various types of applications include single/three-phase grid connection, motor traction and battery.

**Single-Phase Grid**

Firstly, two local power modules can be connected in parallel to formulate a single-phase full-bridge transformerless grid-connected inverter as is shown in Fig. 5.3(a). The state space equations in \(ab\) reference frame can be expressed as:

\[
i_{Lfs,ab} = \frac{1}{L_{fs}}I_{1\phi}v_{x,ab} - \frac{1}{L_{fs}}I_{1\phi}v_{Cf,ab} \quad (5.2a)
\]

\[
\dot{v}_{Cf,ab} = \frac{1}{C_f}I_{1\phi}i_{Lfs,ab} - \frac{1}{C_f}I_{1\phi}i_{Lfg,ab} \quad (5.2b)
\]

\[
i_{Lfg,ab} = \frac{1}{L_{fg}}I_{1\phi}v_{Cf,ab} - \frac{1}{L_{fg}}I_{1\phi}v_{g,ab}, \quad (5.2c)
\]

where \(L_{fs}\), \(C_f\) and \(L_{fg}\) are the switch side inductor, capacitor and grid side inductor, respectively,
for the LCL filter. \(i_{Lfs,ab}, v_{Cf,ab}, i_{Lfsg,ab}\) and \(v_{x,ab}\) are the switch side inductor current, capacitor voltage, grid side current and grid voltage for the single-phase grid-connected system, respectively. \(I_{1\phi} \in \mathbb{R}^{2 \times 2}\) is the identity matrix for single-phase grid connection system.

Leveraging the Park and Clarke transformations, the state space equations can be converted to the \(dq0\) reference frame for the central level control:

\[
\begin{align*}
\dot{i}_{Lfs,dq0} &= \frac{1}{L_{fs}} I_{dq0} v_{x,dq0} - \frac{1}{L_{fs}} I_{dq0} v_{Cf,dq0} - \omega S i_{Lfs,dq0} \\
\dot{v}_{Cf,dq0} &= \frac{1}{C_f} I_{dq0} i_{Lfs,dq0} - \frac{1}{C_f} I_{dq0} i_{Lfsg,dq0} - \omega S v_{Cf,dq0} \\
\dot{i}_{Lfsg,dq0} &= \frac{1}{L_{fg}} I_{dq0} v_{Cf,dq0} - \frac{1}{L_{fg}} I_{dq0} v_{g,dq0} - \omega S i_{Lfsg,dq0}
\end{align*}
\]  

(5.3)

where \(\omega\) is the angular velocity of the grid in rad/s. \(S\) is the matrix, \([0, -1, 0; 1, 0, 0; 0, 0, 0]\), for the coupling terms of single-phase grid-connection model. \(I_{dq0} \in \mathbb{R}^{3 \times 3}\) is the identity matrix for \(dq0\) grid connection system.

Different from the conventional inverter topologies, the upper/lower output capacitors of the local MPC-based power module provide common-mode leakage current bypassing paths for the formulated single-phase grid-connected inverter as is shown in Fig. 5.4(a). The common-mode voltage of the single-phase topology can be derived as:

\[
v_{cm,1\phi} = v_{Cf0,1\phi} = \frac{v_{Cf,a} + v_{Cf,b}}{2}.
\]  

(5.4)

The leakage leakage current is typically excited by the high frequency fluctuation of the common-mode voltage to be injected into the grid through a parasitic capacitor, \(C_{para}\). The leakage current is defined as:

\[
i_{lkg,1\phi} = i_{Lfsg0,1\phi} = C_{para} \frac{dv_{Cf0,1\phi}}{dt}.
\]  

(5.5)

With two MPC-based power modules connected in parallel for single-phase grid-connected inverter in Fig. 5.3(a), the equivalent common-mode circuit in Fig. 5.4(a) demonstrates that the
leakage current can be bypassed by the upper/lower output capacitors with the zero-sequence voltage MPC control. From the control perspective, the embedded local power module zero-sequence voltage MPC can stabilize the common-mode voltage, \( v_{Cf,0,1\phi} \), to be constant as half of DC bus voltage. Then, according to (5.5), the leakage current flowing to the grid will be largely attenuated.

**Three-Phase Grid**

Secondly, three local power modules can be connected in parallel to formulate a three-phase transformerless grid-connected inverter as is shown in Fig. 5.3(b). The state space equations in \( abc \) reference frame is similar with equation (5.2) by substituting \( i_{Lfs,ab}, v_{Cf,ab}, i_{Lfg,ab}, v_{x,ab} \) and \( I_{1\phi} \in \mathbb{R}^{2\times2} \) with \( i_{Lfs,abc}, v_{Cf,abc}, i_{Lfg,abc} \) and \( v_{x,abc} \) and \( I_{3\phi} \in \mathbb{R}^{3\times3} \) for the three-phase system.

Leveraging the Park and Clarke transformations, the state space equations of three-phase system can be converted to the \( dq0 \) reference frame for the central level control which are similar with equation (5.3) in the single-phase system.

Different from the conventional three-phase inverter topologies, the upper/lower output capacitors of the local MPC-based power module provide common-mode leakage current bypassing paths for the formulated three-phase grid-connected inverter as is shown in Fig. 5.4(b). The common-mode voltage and leakage current expressions are similar to equations (5.4) and (5.5) by transferring single-phase variables into three-phase system.

With three MPC-based power modules connected in parallel for three-phase grid-connected inverter in Fig. 5.3(b), the equivalent common-mode circuit in Fig. 5.4(b) demonstrates that the leakage current can be bypassed by the upper/lower output capacitors with the zero-sequence voltage MPC control. From the control perspective, the embedded local power module zero-sequence voltage MPC can stabilize the common-mode voltage, \( v_{Cf,0,3\phi} \), to be constant as half of DC bus voltage. Then, the leakage current flowing to the grid will also be largely attenuated.
Motor Drive

Thirdly, three local power modules can also be connected in parallel to formulate a three-phase transformerless motor traction inverter as is shown in Fig. 5.3(c). Different from the grid-connected inverter applications, the motor drive interface does not require the grid side inductors, $L_{fg}$. Three power modules can be directly connected to the motor. Thus, the motor drive modeling can be separated into switch side $LC$ filter modeling and PMSM modeling.

For the switch side $LC$ filter modeling, the state space equations in $abc$ reference frame can be derived as:

\[
\begin{align*}
\dot{i}_{Lfs,abc} &= \frac{1}{L_{fs}}I_3\phi v_{x,abc} - \frac{1}{L_{fs}}I_3\phi v_{Cf,abc} \\
\dot{v}_{Cf,abc} &= \frac{1}{C_f}I_3\phi i_{Lfs,abc} - \frac{1}{C_f}I_3\phi i_{motor,abc}
\end{align*}
\]  

(5.6a) (5.6b)

where $i_{motor,abc}$ is the current flowing into the motor winding. Leveraging the Park and Clarke transformations, the state space equations can be converted to the $dq0$ reference frame for the central level control:

\[
\begin{align*}
\dot{i}_{Lfs,dq0} &= \frac{1}{L_{fs}}I_{dq0}v_{x,dq0} - \frac{1}{L_{fs}}I_{dq0}v_{Cf,dq0} - \omega M_i_{Lfs,dq0} \\
\dot{v}_{Cf,dq0} &= \frac{1}{C_f}I_{dq0}i_{Lfs,dq0} - \frac{1}{C_f}I_{dq0}i_{motor,dq0} - \omega v_{Cf,dq0}
\end{align*}
\]  

(5.7a) (5.7b)

where $M$ is the matrix, $[0, -1, 0; 1, 0, 0; 0, 0, 0]$, for the coupling terms of motor drive model.

For the motor side modeling, a typical PMSM is analyzed in this section [110]. Different from the grid side inductor current, $i_{Lfg,dq0}$, the motor winding current, $i_{motor,dq0}$, can be modeled as:

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\[ i_{\text{motor},d} = \frac{1}{L_d} (v_{C_f,d} - R_s i_{\text{motor},d} + \omega_e L_d i_{\text{motor},q}) \] (5.8a)

\[ i_{\text{motor},q} = \frac{1}{L_q} (v_{C_f,q} - R_s i_{\text{motor},q} - \omega_e (L_d i_{\text{motor},d} + \psi)) \] (5.8b)

\[ T_e = \frac{3}{2} p (\lambda i_{\text{motor},q} + (L_d - L_q) i_{\text{motor},d} i_{\text{motor},q}) \] (5.8c)

\[ \omega_e = \frac{1}{J} (-B \omega_e + p T_e - p T_l) \] (5.8d)

where \( L_d, L_q \) represent the \( dq \) component inductance of the motor, respectively; \( R_s \) is the stator winding resistance. \( \psi \) is the flux of the permanent magnets. \( \omega_e \) is the electrical angular velocity of the rotor which is related to the mechanical angular velocity \( \omega_m \) by the pole pairs \( p_p \) by \( \omega_e = p_p \omega_m \). \( T_e \) and \( T_l \) are the electrical and load torques, respectively. \( B \) and \( J \) are the friction and inertia coefficients, respectively.

The motor bearing current and shaft voltage caused by the switching pulsation of the traction inverter is a key factor that could result in electric motor failure. The upper/lower output capacitors of the local MPC-based power module can provide common-mode leakage current bypassing paths for the formulated motor traction inverter as is shown in Fig. 5.4(c). The common-mode voltage of the motor traction inverter topology which is highly related to the shaft voltage of the motor can be derived as:

\[ v_{\text{cm,motor}} = v_{C_f0,motor} = \frac{v_{C_f,a} + v_{C_f,b} + v_{C_f,c}}{3} \] (5.9)

For the motor system, the leakage current is also typically generated by the high frequency fluctuation of the common-mode voltage to be injected into the motor bearing through the parasitic capacitor, \( C_{\text{para}} \). The equivalent parasitic circuit model for the motor system has been displayed in Fig. 5.4(c) which consists of two paths. The first parasitic path is from the stator windings to the frame of the motor, \( C_{w2f} \). The second path includes two cascaded sections which are from the stator windings to the rotor, \( C_{w2r} \), and then from the rotor to the frame, \( C_{r2f}, C_{b,NDE}, C_{b,DE} \). The leakage current, \( i_{lk^g,motor} \), generated by the high frequency fluctuation of the common mode volt-
age mainly flows through the first path of stator windings to the frame capacitor, \( C_{w2f} \), because of its low impedance. And the second path of leakage current is mostly relevant to the bearing current and bearing voltage which are also generated by the high frequency fluctuation of common mode voltage. Specifically, \( C_{w2r} \), \( C_{r2f} \), \( C_{b, NDE} \) and \( C_{b, DE} \) are the stator windings to rotor capacitor, rotor to frame capacitor, non-drive end and drive end capacitors, respectively. So, the equivalent parasitic capacitance can be derived as:

\[
C_{para} = \frac{(C_{r2f} + C_{b, NDE} + C_{b, DE})C_{w2r}}{(C_{r2f} + C_{b, NDE} + C_{b, DE}) + C_{w2r}} + C_{w2f} \quad (5.10)
\]

Thus, the leakage current also regarded as the bearing current is defined as:

\[
i_{i_{kg, motor}} = i_{0, motor} = C_{para} \frac{dV_{Cf0, motor}}{dt}. \quad (5.11)
\]

With three MPC-based power modules connected in parallel for the modified motor traction inverter in Fig. 5.3(c), the equivalent common-mode circuit in Fig. 5.4(c) demonstrates that the leakage current can be bypassed by the upper/lower output capacitors with the zero-sequence voltage MPC control. From the control perspective, the embedded local power module zero-sequence voltage MPC can stabilize the motor common-mode voltage, \( V_{Cf0, motor} \), to be constant as half of DC bus voltage. Then, according to (5.11), the leakage current flowing to the motor bearing will also be largely attenuated.

### 5.2 Hierarchical Control Structure

The proposed hierarchical control structure is illustrated in this section. As is demonstrated in Fig. 5.1, the hierarchical control structure consists of three layers: (1) Central control layer for recognition of different types of load/source, reconfiguration of power converter topologies with desired number of power modules, high level current/voltage/power control and generate references for local MPC-based power module control; (2) Local module control layer for implementing the MPC algorithm to track the references from the central controller with improved dynamic performance, stabilizing the common-mode voltage, collecting ADC samplings and generating
Figure 5.3: (a) Single-phase grid (b) three-phase grid and (c) three-phase motor traction topological applications of the multi-layer control architecture.

Figure 5.4: Equivalent common-mode circuit of the formulated (a) Single-phase grid (b) three-phase grid and (c) three-phase motor inverters.
Figure 5.5: (a) Single-phase and (b) three-phase PLL control blocks.

PWM signals for local power switches; (3) Application layer for the interface with different types of load/source including single/three-phase grid, battery, motor drive and so on.

5.2.1 Single-Phase Grid Interface Control

Fig. 5.6 displays the control architecture for the application of single-phase grid interface. The corresponding power converter topology is shown in Fig. 5.3(a).

Central Control Layer

The central control layer is functioned to recognize the single-phase grid interface and reconfigure the power converter topology with two local power modules in parallel as is shown in Fig. 5.3(a). The specific functions of single-phase grid interface central control layer are illustrated as follows.

Firstly, the single-phase grid side inductor current, \( i_{Lfg,ab} \), and output capacitor voltage, \( v_{Cf,ab} \), are received from the local power modules and transformed into \( dq0 \) reference frame as \( i_{Lfg,dq0} \) and \( v_{Cf,dq0} \), respectively, for the high level control purpose.

Secondly, the single-phase phase-lock loop (PLL) is designed in the central control layer as is shown in Fig. 5.5(a). The virtual \( \alpha \beta \) components of output capacitor voltage are constructed and transformed to \( dq \) axis to control the \( q \) component to be zero for the generation of accurate grid angular speed, \( \omega \), and phase angle, \( \theta \).

Thirdly, the grid service control functions are configured to provide active/reactive power com-
pensations based on the grid frequency/voltage abnormal conditions. The grid service control blocks are detailed in Fig. 5.9 by following the standardized principles of IEEE 1547 [111]. The general implementing methodology is to output the certain amount of active/reactive power for the distributed energy resources (DER) by following the prescribed linear curve functions. The linear functions in the grid service standards regulate the output active/reactive power based on the variations of grid voltage/frequency and output active power to compensate for the abnormal grid
conditions. Six typical working modes of the grid services have been shown in Fig. 5.9 including constant reactive power mode (Const-Var), constant power factor mode (Const-PF), grid voltage and reactive power mode (Volt-Var), active power and reactive power mode (P-Q), grid frequency and active power mode (Freq-Watt), grid voltage and active power mode (Volt-Watt). Thus, the grid service controller in the central control layer receives the measured grid voltage/frequency and active power of DER to generate the desired active/reactive power references, $P^*$ and $Q^*$, for the active/reactive power controllers. The active/reactive power controllers derive the $dq$ components of grid side inductor current references, $i_{Lg,dq}^*$, for the following grid current $dq$ controllers.

Fourthly, the grid side inductor current $dq$ components, $i_{Lg,dq}$, are controlled separately with
two PI controllers to generate $dq$ output capacitor voltage references, $v_{Cf,dq}^\ast$. And the zero-sequence output capacitor voltage reference, $v_{Cf,0}^\ast$, is configured as half of DC bus voltage, $v_{dc}$, to stabilize the common mode voltage. Combining the zero-sequence voltage control with the modified topology in Fig. 5.3(a), the leakage current can be attenuated from flowing into the grid.

Then, the $dq0$ components of output capacitor voltage references are transformed into $ab$ reference frame with the reversed Park and Clarke functions as, $v_{Cf,ab}^\ast$. The generated $v_{Cf,ab}^\ast$ will then be distributed to the per phase local module control layer as the tracking references of local MPC control.
Local Module Control Layer

The local module control layer of the single-phase grid interfaced system consists of two MPC-based power modules. Each of the power module is implementing the same MPC algorithm for the switch side $LC$ filter to track the output capacitor voltage reference, $v_{c,f,ab}^*$, received from the central control layer.

For the MPC implementation, in every control period, the MPC controller receives the measured switch side inductor current, $i_{L,abc}$, capacitor voltage, $v_{c,abc}$, grid current, $i_{g,abc}$, from ADC and capacitor voltage reference, $v_{c,abc}^*$ from the grid current controller. An offline generated piecewise affine search tree is applied to derive the optimal duty cycle for the explicit MPC. The discrete state equations of switch side LC filter can be derived from the continuous equations in (5.1) as:
\[
\begin{align*}
    i_{Lf}(k+1) &= i_{Lf}(k) - \frac{T_s}{L_{fs}}v_{Cf}(k) + \frac{v_{dc}T_s}{L_{fs}}d(k) \quad (5.12a) \\
    v_{Cf}(k+1) &= \frac{T_s}{C_f}i_{Lf}(k) + v_{Cf}(k) - \frac{T_s}{C_f}i_{Lf}(k). \quad (5.12b)
\end{align*}
\]

For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the DC bus voltage during test, the last term of (5.12), \(v_{dc}d(k)\), can be replaced by the phase leg output voltage, \(v_x(k)\). The state-space model for MPC can be expressed in standard matrix format of

\[
X_{k+1} = A_CX_k + B_Cu_k + E_Ce_k \quad (5.13)
\]

where the variables and matrices for MPC control represent

\[
\begin{align*}
    A_C &= \begin{bmatrix} 1 & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix},
    B_C &= \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix},
    E_C &= \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix}, \quad (5.14a) \\
    X_k &= \begin{bmatrix} i_{Lf}(k) \\ v_{Cf}(k) \end{bmatrix},
    u_k &= \begin{bmatrix} v_{dc}(k) \end{bmatrix},
    e_k &= \begin{bmatrix} i_{Lf}(k) \end{bmatrix}. \quad (5.14b)
\end{align*}
\]

In the MPC formulation, the inductor current/capacitor voltage references can be defined as \(\bar{X}\) and the tracking errors between the measurement and the references are expressed as \(\tilde{X}\) which are composed of

\[
\begin{align*}
    \bar{X}_k &= \begin{bmatrix} i_{Lfs,ref}(k) \\ v_{Cf,ref}(k) \end{bmatrix},
    \tilde{X}_k &= \begin{bmatrix} i_{Lfs,ref}(k) - i_{Lfs}(k) \\ v_{Cf,ref}(k) - v_{Cf}(k) \end{bmatrix}. \quad (5.15)
\end{align*}
\]

Thus, the cost function includes two terms

\[
\min_k \sum_{k=0}^{N_c} \tilde{X}_k^TQ_C\tilde{X}_k + \sum_{k=0}^{N_p-1} \Delta u_k^TR_C\Delta u_k. \quad (5.16)
\]
For the penalties of the MPC cost function, $Q_C$ and $R_C$ represent the weighing factor matrices that are implemented on the state values and input values, respectively.

**Application Layer**

For the application layer, the interface between the local power modules and the single-phase grid are two grid side inductors, $L_{fg}$.

5.2.2 Three-Phase Grid Interface Control

Fig. 5.7 displays the control architecture for the application of three-phase grid interface. The corresponding power converter topology is shown in Fig. 5.3(b).

**Central Control Layer**

The central control layer is functioned to recognize the three-phase grid interface and reconfigure the power converter topology with three local power modules in parallel as is shown in Fig. 5.3(b). The specific functions of three-phase grid interface central control layer are illustrated as follows.

Firstly, the three-phase grid side inductor current, $i_{L_{fg},abc}$, and output capacitor voltage, $v_{Cf,abc}$, are received from the local power modules and transformed into $dq0$ reference frame as $i_{L_{fg},dq0}$ and $v_{Cf,dq0}$, respectively, for the high level control purpose.

Secondly, the three-phase PLL is designed in the central control layer as is shown in Fig. 5.5(b). The $abc$ components of output capacitor voltage are received from local power modules and transformed to $dq$ axis to control the $q$ component to be zero for the generation of accurate grid angular speed, $\omega$, and phase angle, $\theta$.

Thirdly, the grid service control functions are configured to provide active/reactive power compensations based on the grid frequency/voltage abnormal conditions. The grid service control blocks are also following the working modes in Fig. 5.9 to generate the desired active/reactive power references, $P^*$ and $Q^*$, for the active/reactive power controllers. The active/reactive power
controllers derive the \( dq \) components of grid side inductor current references, \( i_{Lfg,dq}^* \) for the following grid current \( dq \) controllers.

Fourthly, the grid side inductor current \( dq \) components, \( i_{Lfg,dq0} \), are controlled separately with two PI controllers to generate \( dq \) output capacitor voltage references, \( v_{Cf,dq}^* \). And the zero-sequence output capacitor voltage reference, \( v_{Cf,0}^* \), is configured as half of DC bus voltage, \( v_{dc} \), to stabilize the common mode voltage. Combining the zero-sequence voltage control with the modified topology in Fig. 5.3(b), the leakage current can be attenuated from flowing into the grid. Then, the \( dq0 \) components of output capacitor voltage references are transformed into \( abc \) reference frame with the reversed Park and Clarke functions as, \( v_{Cf,abc}^* \). The generated \( v_{Cf,abc}^* \) then will be distributed to the per phase local module control layer as the tracking references of local MPC control.

**Local Module Control Layer**

The local module control layer of the three-phase grid interfaced system consists of three MPC-based power modules. Each of the power module is implementing the same MPC algorithm for the switch side \( LC \) filter to track the output capacitor voltage reference, \( v_{Cf,abc}^* \), received from the central control layer.

**Application Layer**

For the application layer, the interface between the local power modules and the three-phase grid are three grid side inductors, \( L_{fg} \).

5.2.3 Motor Drive Interface Control

Fig. 5.8 illustrates the control architecture for the application of motor drive. The corresponding motor traction inverter topology is shown in Fig. 5.3(c). A permanent magnet synchronous motor (PMSM) is connected directly to the three local MPC-based power modules for the validation.
**Central Control Layer**

The central control layer is functioned to recognize the motor interface and reconfigure the power converter topology with three local power modules in parallel as is shown in Fig. 5.3(c). The specific functions of motor interface central control layer are illustrated as follows.

Firstly, the rotor position is measured with an encoder board. And a speed controller is designed to control the rotor speed. The output of the speed controller is configured as the $q$ component motor winding current reference, $i_{motor,q}$ to be cascaded with the following motor current controllers.

Secondly, the three-phase motor winding current, $i_{motor,abc}$, and output capacitor voltage, $v_{Cf,abc}$, are received from the local power modules and transformed into $dq0$ reference frame as $i_{motor,dq0}$ and $v_{Cf,dq0}$, respectively, for the high level control purpose.

Thirdly, the motor winding current $dq$ components, $i_{motor,dq}$, are controlled separately with two PI controllers to generate $dq$ output capacitor voltage references, $v_{Cf,dq}^*$. And the zero-sequence output capacitor voltage reference, $v_{Cf,0}^*$, is configured as half of DC bus voltage, $v_{dc}$. Then, the $dq0$ components of output capacitor voltage references are transformed into $abc$ reference frame with the reversed Park and Clarke functions as, $v_{Cf,abc}^*$. The generated $v_{Cf,abc}^*$ then will be distributed to the per phase local module control layer as the tracking references of local MPC control.

**Local Module Control Layer**

The local module control layer of the motor interfaced system consists of three MPC-based power modules. Each of the power module is implementing the same MPC algorithm for the switch side $LC$ filter to track the output capacitor voltage reference, $v_{Cf,abc}^*$, received from the central control layer.

**Application Layer**

For the application layer, the three local power modules are directly interfaced with the PMSM.
5.3 Merits and Validations

The proposed hierarchical software-defined control architecture is validated experimentally on the MPC-based power module test bench with C3M0021120K MOSFETs and TMS320F280049 control card configured with CAN communication as is shown in Fig. 5.10. The merits of the designed architecture can be concluded in the following four aspects.

5.3.1 Reconfigurability with Unified Power Modules

Firstly, one of the major merits for the proposed hierarchical control architecture is the reconfigurability to be applied to different applications with the unified MPC-based power modules. As is shown in Fig. 5.1 and 5.10, different number of MPC-based power modules can be connected to formalize the desired circuitry topology and interfaced application. Fig. 5.11(a) and 5.11(b) show the single- and three-phase grid interfaced applications of the grid current, capacitor voltage, inductor current and DC voltage waveforms, respectively. The testing results of motor application are shown in Fig. 5.12(a) and 5.12(b) with speed step of 730 rpm and torque step of 26 Nm, respec-
Figure 5.11: (a) Single-phase and (b) Three-phase grid interfaces grid current, capacitor voltage, inductor current and DC voltage steady state waveforms.

Figure 5.12: Captured ADC readings of motor (a) speed step from 0 to 470 rpm and (b) torque step from 5 to -5 Nm.

tively. The three applications, single/three-phase grid and motor, are all following the hierarchical control architectures illustrated in Fig. 5.6, 5.7 and 5.8, respectively.
5.3.2 Improved Dynamic Performance with MPC-Based Local Layer Power Module

Secondly, the local level MPC control improves the dynamic performance by actively damping the resonance of the $LCL$ filter and enabling a high control bandwidth. By inserting an MPC loop between the central level output current PI and PWM modulation, the control gain is capable of being largely increased without inducing too much resonant oscillation. Fig. 5.13(a) and 5.11(b) shows the single- and three-phase grid interfaced applications of the grid current, capacitor voltage, inductor current and DC voltage waveforms, respectively, with current step from 2A to 6A. Also,
Figure 5.15: The comparison of leakage current and common mode voltage for the (a) proposed grid connected topology with zero-sequence voltage control (c) proposed three-phase grid connected topology without zero-sequence voltage control and (d) traditional topology without zero-sequence voltage control.

Figure 5.16: The comparison of leakage current, shaft voltage and common mode voltage for the (a) conventional motor connected topology (b) proposed motor connected topology with zero-sequence voltage control.

for a better comparison with the conventional PI control, three testing cases of the captured ADC readings for grid current from 2A to 8A and 8A to 2A are shown in Fig. 5.14(a) and 5.14(b), respectively. Compared with low $K_p$ of the traditional PI, the proposed MPC control can track the reference 5 times faster without overshoot. Compared with high $K_p$ of the traditional PI, the proposed MPC control performs more steadily without oscillation.
5.3.3 Non-Isolated Applications with Central Layer Zero-Sequence Control

Thirdly, the central layer manages a zero-sequence voltage control to be distributed to the local MPC power modules. With the zero-sequence controller combined with the modified topologies in Fig. 5.4(a), 5.4(b) and 5.4(c), the leakage current/common mode voltage of single/three-phase grid and shaft voltage/bearing current of motor can be attenuated. Thus, the non-isolated topology can save the cost of bulky transformer. Specifically, Fig. 5.15(a)-5.15(c) compare the leakage current and common mode voltage for the modified grid-connected topology with zero-sequence controller, the modified grid-connected topology without zero-sequence controller and conventional grid-connected topology without zero-sequence controller, respectively. Only leveraging the modified topologies can reduce 2-3 times leakage current. However, combining the modified topologies with zero-sequence controller can reduce 10-15 times leakage current. Also, the comparison of leakage current, shaft voltage and common mode voltage for the conventional motor connected topology and proposed motor connected topology with zero-sequence voltage control in Fig. 5.16 demonstrates that the leakage current and shaft voltage on the motor can be attenuated by 10-20 times.

5.3.4 Robust MPC Free of Application Model Parameters Influence

Lastly, for the proposed hierarchical control architecture, the control accuracy and robustness are guaranteed by the cascaded multi-layer control structure. As are shown in Fig. 5.6, 5.7 and 5.8 of the three applications, the output side inductor current is directly managed by the central layer controller and the corresponding output side inductance is free from the local MPC parametric modeling. Thus, the uncertainties of the equivalent output parameters caused by the various interfaced grid or motor will not influence the accuracy of the local MPC parametric modeling.
5.4 Summary

This chapter develops a hierarchical software-defined control architecture with MPC-based power module to improve the performance of energy conversion system. The multi-layer control structure includes central control layer for high-level power control, local MPC control layer for each power module and application layer for different interfaces. Different applications have been demonstrated to be applied in the generalized control architecture such as single/three-phase grid and motor. The developed structure has the advantages of reconfigurability for various application requirements, better transient performance improved by the local MPC modules, non-isolated topologies enabled by the central level zero-sequence control and high accuracy free from the parameter uncertainties of different interfaces.
Chapter 6: Design Case of Three-Phase Grid-Tied Inverter with High Efficiency and Power Density

With the increasing demands of high efficiency, high power density and better dynamic/steady state performance in the application of power electronics, more advanced control techniques and circuitry topologies have been studied to improve the performance of power converters. To achieve high power density with low volume, the size of passive magnetic components needs to be reduced. Thus, it is necessary to increase the switching frequency for maintaining reasonable current/voltage ripples on the inductor/capacitor [112], [113]. However, higher switching frequency brings more switching losses and inductor losses which could influence the efficiency of the power conversion system. Thus, there exists a typical trade-off between efficiency and power density for balancing [114]. For the dynamic performance of power converters, besides a careful hardware design, more advanced control techniques can contribute to the transient behavior. Model predictive control (MPC) has been studied to have better dynamic performance than the traditional method of PI control [75].

Firstly, for the trade-off between high efficiency and high power density, soft switching techniques can be applied to achieve both targets with less compromise [115]. The switching losses are mainly caused by the overlapping of voltage and current across the switch during turn-on and turn-off transients. Soft switching techniques are generally aimed at minimizing the overlapping area of switch voltage and current in transients. Zero-voltage switching (ZVS) and zero-current switching (ZCS) are the two main soft switching methods [116], [117]. ZVS focuses on reducing the voltage across the switch and ZCS can minimize the current flowing through the switch during the turn-on or turn-off transients [118], [119]. The soft switching can be achieved by adding auxiliary circuit. Typically, extra inductor, capacitor and switch are needed to form the buffer circuit.
for the implementation of soft switching [120], [121]. This will bring extra cost and control complexity. Another method to achieve ZVS is by replacing the higher turn-on loss with lower turn-off loss. This strategy can be realized by controlling the switch side inductor current ripple to be bidirectional during switching transients [122]. To control the peak/valley inductor current for ZVS, the simplest way is varying the switching frequency for the adjustment of inductor current ripple [123]. A variable frequency soft switching method is proposed in this chapter in combination with MPC and state estimator to reduce the switching losses without introducing auxiliary circuit.

Secondly, for the improvement of dynamic performance, advanced control techniques can be applied. Different from the conventional proportional and integral (PI) control method, model predictive control (MPC) has the advantages in the aspects of rising time, overshoot and disturbance rejection [76]. The MPC is typically implemented by optimizing the tracking error between the measurement and reference in the desired future steps to predict the duty cycle for the modulation [77]. Some recent MPC techniques have been published to improve the performance of inverter control [124, 125, 126, 127]. Specifically, [124] leveraged joint voltage vector for the Quazi-Z-Source inverter MPC control to suppress the current ripple. [125] developed the constrained MPC algorithm based on large-signal model for microgrid inverter. [126] proposed a voltage-sensorless MPC for grid-connected inverter. And [127] enabled the MPC control with inductance online identification capability and improved phase-locked loop. The MPC can perform a high tracking speed with less transient oscillation especially during load or reference variations [43]. This characteristic can be combined with the variable frequency soft switching technique to reduce the oscillation caused by the switching frequency variation. The design case in this chapter leverages the advantages of MPC in dynamic performance to mitigate the oscillation and stability issue caused by the variable frequency soft switching operation.

Thirdly, for the accuracy of state parameter acquisition, the state estimation techniques have been developed to improve the quality of sampling information and reduce the sensor cost. The recent publications are introduced as follows. Specifically, in the power electronics field, [128] developed a state and disturbance observer for grid-connected inverter under non-ideal conditions.
[129] proposed a robust observer algorithm for Voltage and frequency control of a doubly fed induction generator. [130] applied an extended-state observer estimation method for \( LCL \) inverter to improve the observation dynamics. [131] studied the resonant extended state observer for grid voltage estimation of \( LCL \) inverter.

The contributions of this chapter can be concluded in four main aspects. Firstly, the combination of MPC with variable-frequency critical-soft-switching control improves the efficiency of grid-connected inverter. The unexpected hard switching power loss from the oscillation caused by the time-varying switching frequency is attenuated by the MPC due to the robust transient performance. Secondly, two variable-frequency techniques, VCF-CSS and VDF-CSS, are proposed to achieve the full grid period soft switching. A Luenberger Observer is designed to be integrated with VCF-CSS for a more accurate inductor current estimation and soft switching boundary calculation. Both VCF-CSS and VDF-CSS do not need extra sensor circuits, e.g., [132], to sample the averaged inductor current for soft switching. Thirdly, the zero-sequence voltage control method combined with the modified inverter topology enables the non-isolated circuitry application with low leakage current. Fourthly, compared with the typical prototypes, the designed inverter achieves the Pareto Optimal Points in the parameters of Frequency-Power and Efficiency-Power density.

This chapter is organized as follows. Firstly, a modified non-isolated grid connected inverter topology is introduced. The modified topology is composed based on a fundamental power module for each phase. The power module includes upper/lower switches, switch side inductor and two output capacitors to be connected to the upper/lower DC bus terminals. Three power modules can be connected to form a modified three phase non-isolated inverter with the capability to stabilize the zero-sequence voltage and attenuate the leakage current. Then, based on the power module, a critical soft switching technique is introduced to reduce the large turn-on loss with small turn-off loss for the improvement of efficiency. Thirdly, the control strategies are proposed including three parts: (1) central level of grid current control/zero-sequence voltage control cascaded with local level of per phase power module modular model predictive control; (2) two types of variable-frequency critical-soft-switching controllers including variable-continuous-frequency critical-soft-
switching (VCF-CSS) and variable-discrete-frequency critical-soft-switching controllers (VDF-CSS) to achieve highly efficient critical soft switching operation by adjusting switching frequency and inductor current ripple; (3) state estimator for per power module to estimate the switch side inductor current, output capacitor voltage and grid side inductor current with the sampling values of output capacitor voltage and grid side inductor current. The combination of MPC and VF-CSS guarantees a complete critical soft switching operation at full period range of varying frequency and especially during transient. The estimator provides noise rejection and accurate switch side inductor current estimations for MPC and VF-CSS. Three controllers can be combined to achieve a high efficiency, good dynamic/steady state performance non-isolated grid-tied inverter with low leakage current. Finally, two cases of prototype are built with medium frequency/medium inductance (>200kHz, 45\(\mu\)H) and high frequency/small inductance (>1MHz, 4.5\(\mu\)H) to validate the effectiveness of the proposed methods. The efficiency is above 99% at a rated power of 15kW. A power density of more than 10.4kW/L is achieved.
6.1 Non-Isolated System and Critical Soft Switching

6.1.1 Non-isolated System

The proposed control methods are based on a modified non-isolated grid-tied \( LCL \) inverter. Different from the conventional \( L \) and \( LCL \) types of non-isolated inverters in Fig. 6.1, the proposed topology is shown in Fig. 6.2 which consists of three power module units and three grid side inductors, \( L_{fg} \). The per phase power module unit is composed of upper/lower switches, \( M_1 \) and \( M_2 \), switch side inductor, \( L_{fs} \), and two output capacitors connected to the upper/lower DC bus terminals, \( C_{f,up} \) and \( C_{f,lo} \). The modification of non-isolated topology contributes to the stabilization of common mode voltage leveraging the proposed control methods and the proposed variable-frequency critical-soft-switching methods, VCF-CSS and VDF-CSS, are based on the per phase power module unit. As is shown in Fig. 6.2, the local level control is implemented at each of the power module independently for MPC, estimator and VF-CSS to improve the efficiency and dynamic/steady state performance.

The modified non-isolated topology is composed of three power modules (upper/lower switches, switch side inductor, upper/lower capacitors), grid side inductors and DC bus capacitor as is shown in Fig. 6.2. With the help of the power module units labeled in colored blocks in Fig. 6.2, the upper/lower common points of three-phase output capacitors are connected to the positive/negative DC bus terminals, respectively. This topological modification allows the zero-sequence capacitor voltage to be stabilized as constant and the leakage current to be bypassed from flowing into the grid.

6.1.2 Critical Soft Switching Analysis

To reduce the switching losses of the power module, a critical soft switching method is introduced in this section. The critical soft switching technique is aimed at improving the power density and efficiency at the same time. It permits to increase the switching frequency by a factor of 3-5 and reduce the required inductance by a factor of 10-20. As is shown in Fig. 6.3, three sets of
inductors are compared in size and volume with the inductance of 450\(\mu\)H, 45\(\mu\)H and 4.5\(\mu\)H, respectively. From left to right of the three inductors, the inductance are decreased by a factor of 10 in sequence, the volume is decreased by the factors of 5.5 and 4.1 in sequence, respectively. For the inductor design perspective considering the area product (AP), losses and current ripple saturation, the desired operating frequencies are increased by a factor of 3-5 from left to right in sequence. Thus, instead of using a bulky 450\(\mu\)H inductor on the left side of Fig. 6.3 for hard switching, the critical soft switching technique enables smaller inductors on the middle and right sides of Fig. 6.3 with lower inductance-switching losses and higher switching frequency/power density.
Figure 6.5: Turn-on and turn-off loss comparison of typical SiC MOSFET C3M0021120K.

The working principle diagram of critical soft switching is shown in Fig. 6.4 with DC and AC current modes for each of the proposed power module. The core idea of critical soft switching method is to replace the large turn-on loss of the upper switch with small turn-off loss of the lower switch in the power module. For a typical SiC MOSFET, C3M0021120K, at a certain DC voltage of 800V, the turn-on, turn-off and total switching losses of energy have been plotted in Fig. 6.5 with the drain-source current which shows that the turn-on loss is 4 times larger than the turn-off loss. The methodology of critical soft switching is to ensure that the peak point and valley point of the switch side inductor current should be positive and negative, respectively. And the absolute values of positive peak point and negative valley point should be above a threshold current level to ensure the complete soft switching. The threshold current and dead time define the boundary

Figure 6.6: The critical soft switching operation regions for different devices.
condition of critical soft switching. As is shown in Fig. 6.4, in the turn-on transient of upper switch, a negative inductor current can discharge the upper switch output capacitor, $C_{oss,M1}$. The zero-voltage turn-on of upper switch will be achieved if $C_{oss,M1}$ is fully discharged before it turns on. Similarly, a positive inductor current is needed to fully discharge the lower switch output capacitor, $C_{oss,M2}$, before it turns on. The critical soft switching deals with the boundary condition of zero-voltage soft turn-on for the required threshold current and dead time to fully discharge the output capacitors of upper and lower switches before they turn on. The DC and AC current modes of switch side inductor current waveforms have been shown at the bottom of Fig. 6.4 where the dashed lines of current ripple envelope demonstrate the required threshold current for critical soft switching operation at certain dead time.

The switch side inductor current peak/valley point values, $i_{Lfs,max/\text{min}}$, for critical soft switching operation can be expressed by the drain-source current through the upper and lower switches, $i_{DS,M1}$ and $i_{DS,M2}$, and the current through the upper and lower switch output capacitance, $i_{CDS,M1}$ and $i_{CDS,M2}$. And the $i_{CDS,M1}$ and $i_{CDS,M2}$ are the derivative functions of upper/lower switch output capacitors, $C_{DS,M1}$ and $C_{DS,M2}$, and drain-source voltages, $v_{DS,M1}$ and $v_{DS,M2}$. Then, with the integral calculation in each switching dead time period, $t_d$, the required $i_{Lfs,max/\text{min}}$ at specific dead time can be further expressed by the discharge, $Q_{\text{min}}$ and $Q_{\text{max}}$, of upper/lower switch output capacitors which have been provided by the MOSFET manuals:

$$\frac{1}{2}i_{Lfs,\text{min}}t_d \leq Q_{\text{min}} \leq 0 \quad (6.1a)$$

$$\frac{1}{2}i_{Lfs,\text{max}}t_d \geq Q_{\text{max}} \geq 0 \quad (6.1b)$$

Then, the model of critical soft switching method can be expressed with the function image in Fig. 6.6 where the light green regions are the feasible soft switching range based on (6.1) and the peak/valley inductor current can be controlled with the developed methods in the following sections.
6.2 Control

The proposed control strategies of the modified non-isolated converter include two layers of control: (1) Central level grid side inductor current control and zero-sequence voltage MPC control to generate the references for the per phase power module local control; (2) Local level per power module model predictive control, state estimator and variable-frequency critical-soft-switching control. The combination of MPC and VF-CSS guarantees a complete critical soft switching operation at varying frequency and even transient. The state estimator provides noise rejection and more accurate switch side inductor current estimations for MPC and VF-CSS.

6.2.1 Central Level Grid Current/Zero-Sequence Voltage Control

As is shown in the left block of Fig. 6.7, the central level control layer is composed of phase-lock-loop (PLL), Park/Clarke transformations, grid current control and zero-sequence voltage control. Two main targets are achieved with central level grid current and zero-sequence voltage control: (1) provide the three-phase capacitor voltage references for local level power module MPC control; (2) stabilize the zero-sequence voltage and attenuate the leakage current for the modified
non-isolated topology.

**Grid side inductor current control**

The three-phase grid side inductor currents are transformed from $abc$ to $dq0$ reference frame with PLL and Clarke/Park transformations. Two PI controllers are designed to regulate the $d$ and $q$ components of grid current, $i_{Lfg,d}$ and $i_{Lfg,q}$, respectively. The outputs of $dq$ grid current controllers are configured as the $dq$ output capacitor voltage references, $V_{c,d}^*$ and $V_{c,q}^*$, respectively. Then $V_{c,d}^*$ and $V_{c,q}^*$ are transformed to $abc$ reference frame as $V_{c,a}^*$, $V_{c,b}^*$ and $V_{c,c}^*$, for the tracking purpose of per phase local power module MPC control.

**Zero-sequence voltage control**

Based on the proposed topological modification in Fig. 6.2 to connect three-phase output capacitors common points with positive/negative DC bus terminals, the zero-sequence capacitor voltage is controlled to be half of DC bus voltage as is shown in Fig. 6.7. In central level control layer, the zero-sequence output capacitor voltage reference is configured to be half of DC bus voltage and allocated to the local level per phase MPC controller. Thus, the local MPC can stabilize the zero-sequence capacitor voltage to attenuate the leakage current. Since the controlled three-phase output capacitor voltages, $v_{Cf,abc}$, are measured with respect to the DC bus negative terminal and the upper/lower capacitors are connected to the DC bus positive/negative terminals, the output capacitor voltage waveforms will be ranged within $0-V_{dc}$ and centered at $V_{dc}/2$. Thus, the reference of zero-sequence voltage controller is configured as $V_{dc}/2$ for the common mode voltage stabilization.

In the conventional topologies, the zero-sequence capacitor voltage is not controlled to be constant which causes the leakage current to be flowing into the grid. However, in the proposed modified circuit, the zero-sequence capacitor voltage is stabilized by MPC to be half of DC bus. Thus, the zero-sequence current will be bypassed to be only flowing through the switch side inductors. The leakage current will be prevented from injecting into the grid. The definition of leakage
current to the grid can be expressed as:

\[ i_{Lfg,0} = C_p \frac{dV_{c,0}}{dt}. \]  

(6.2)

Thus, the zero-sequence capacitor voltage stabilization by MPC can attenuate the grid side leakage current.
6.2.2 Local Level Model Predictive Control

For the purpose of improving the dynamic performance especially when the controller is combined with variable-frequency operations, an explicit MPC method is designed for the per phase switch side capacitor voltage and inductor current control by solving the *Constrained Finite Time Optimal Control* (CFTOC) problem. As is shown in Fig. 6.7 of the control diagram, the three-phase capacitor voltages are controlled in $abc$ frame to follow the references from the cascaded grid current controller’s outputs. The switch side inductor currents are also regulated with the MPC by adjusting the weighing factor between $i_{Lfs,abc}$ and $v_{Cf,abc}$. The benefits to configure the MPC per phase in $abc$ frame can be concluded as: (1) the state space matrix of LC per phase is simpler than $dq$ system to implement the offline piecewise affine optimization code in a less costly DSP controller; (2) The time-varying angular speed term, $\omega$, in the typical three-phase $LCL$ inverter state space equations can be omitted in the explicit MPC state space matrix for the offline optimization calculation; (3) Per phase MPC for $LC$ is more flexible for a modular design perspective to extend the paralleled phase number and other topologies, e.g., DC/DC, single-phase DC/AC converters.

For the MPC implementation, in every control period, the MPC controller receives the measured switch side inductor current, $i_{Lfs,abc}$, output lower capacitor voltage, $v_{Cf,abc}$, grid current, $i_{Lfg,abc}$, from ADC and capacitor voltage reference, $v_{Cf,abc}^*$ from the grid current controller. An offline generated piecewise affine search tree is applied to derive the optimal duty cycle for the explicit MPC. The equivalent circuit for each power module is shown in Fig. 6.8 with the variables to derive the state space equation for MPC. The state equations of switch side LC filter can be expressed as

\[
i_{Lfs}(k + 1) = i_{Lfs}(k) - \frac{T_s}{L_{fs}} v_{Cf}(k) + \frac{v_{dc} T_s}{L_{fs}} d(k)
\]

\[
v_{Cf}(k + 1) = \frac{T_s}{C_f} i_{Lfs}(k) + v_{Cf}(k) - \frac{T_s}{C_f} i_{Lfg}(k).
\]

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For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the DC bus voltage during test, the last term of (6.3), $v_{dc,d}(k)$, can be replaced by the switch leg output voltage, $v_x(k)$. The state-space model for MPC can be expressed in standard matrix format of

$$X_{k+1} = A_CX_k + B_Cu_k + E_Ce_k$$  \hspace{1cm} (6.4)$$

where the variables and matrices for MPC control represent

$$A_C = \begin{bmatrix} 1 & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix}, B_C = \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix}, E_C = \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix},$$  \hspace{1cm} (6.5a)$$

$$X_k = \begin{bmatrix} i_{L_{fs}}(k) \\ v_{C_f}(k) \end{bmatrix}, u_k = \begin{bmatrix} v_{dc,d}(k) \end{bmatrix}, e_k = \begin{bmatrix} i_{L_{fg}}(k) \end{bmatrix}.$$  \hspace{1cm} (6.5b)$$

In the MPC formulation, the inductor current/capacitor voltage references can be defined as $\bar{X}$ and the tracking errors between the measurement and the references are expressed as $\tilde{X}$ which are composed of

$$\bar{X}_k = \begin{bmatrix} i_{L_{fs,ref}}(k) \\ v_{C_f,ref}(k) \end{bmatrix}, \tilde{X}_k = \begin{bmatrix} i_{L_{fs,ref}}(k) - i_{L_{fs}}(k) \\ v_{C_f,ref}(k) - v_{C_f}(k) \end{bmatrix}.$$  \hspace{1cm} (6.6)$$

Thus, the cost function includes two terms

$$\min \sum_{k=0}^{N_c} \bar{X}_k^T Q_C \bar{X}_k + \sum_{k=0}^{N_p-1} \Delta u_k^T R_C \Delta u_k.$$  \hspace{1cm} (6.7)$$

For the penalties of the MPC cost function, $Q_C$ and $R_C$ represent the weighing factor matrices that are implemented on the state values and input values, respectively.
The constraints of the MPC controller can be expressed as

\[
\tilde{X}_{k+1} = \Lambda \tilde{X}_k + B u_k + E e_k \in \mathcal{X}
\]  

(6.8)

\[
\Delta u_k = u_k - u_{k-1} \in \mathcal{U}
\]  

(6.9)

\[
\begin{bmatrix}
-I_{L,fs,max} \\
0 \\
0 \\
-\text{I}_{L,fg,max}
\end{bmatrix} \leq X_k \leq 
\begin{bmatrix}
I_{L,fs,max} \\
v_{dc} \\
v_{dc} \\
\text{I}_{L,fg,max}
\end{bmatrix}
\]  

(6.10)

\[
\begin{bmatrix}
0 \\
0 \\
0 \\
-\text{I}_{L,fg,max}
\end{bmatrix} \leq u_k \leq 
\begin{bmatrix}
\text{I}_{L,fg,max}
\end{bmatrix}
\]  

(6.11)

\[
\begin{bmatrix}
-\text{I}_{L,fg,max}
\end{bmatrix} \leq e_k \leq 
\begin{bmatrix}
\text{I}_{L,fg,max}
\end{bmatrix}
\]  

(6.12)

Since the application of the MPC is kilo-to-mega-Hertz switching frequency, the execution efficiency of the algorithm should be high. Thus, an explicit method is developed to relieve the online MPC implementation burden. Specifically, based on the state space model, cost function and the corresponding constraints of the power module, a piecewise affine (PWA) function is derived with computer and the related C code is configured in the DSP controller memory for the online implementation. The internal operation principle of the MPC is shown in Fig. 6.9 where the flowchart of MPC implementing process is demonstrated. The PWA function is reflected on the C code as \( n \) sections of active regions, \( H_n \) and \( K_n \), with the corresponding feedback law, \( F_n \) and \( G_n \). And the colored areas in Fig. 6.9 represent different regions. A binary search tree is configured to quickly find the active region, \( r \), and the related feedback law, \( F_r \) and \( G_r \), for the derivation of the optimal duty cycle.

During the control interrupt period, the binary search tree finds the active region, \( r \), based on the ADC samplings/estimations of inductor current, capacitor voltage, output current and the tracking references. Then, the corresponding feedback law, \( F_r \) and \( G_r \), will calculate the optimal duty cycle for PWM modulation. This simplified explicit process avoids the online MPC optimization and is suitable for the developed high frequency inverter control design.
6.2.3 Local Level Luenberger Observer

A state estimator is designed for per phase power module to provide more accurate switch side inductor current estimation and noise rejection as is shown in Fig. 6.10. Since the VF-CSS controller needs an accurate inductor current sampling for peak/valley ripple current calculations especially when the current ripple is huge ($\geq 200\%$), a state estimator is desired to predict the inductor current with capacitor voltage and grid current samplings. The main purposes of the state estimator are (1) avoid inaccuracy of inductor current sampling with high current ripple for VF-CSS; (2) improve the anti-noise capability for better control performance; (3) reduce the sensor cost.

The Luenberger observer is designed to estimate the switch side inductor current, $\hat{i}_{Lfs}$, capaci-
tor voltage, $v_{Cf}$, and grid side inductor current, $i_{Lfg}$, with the samplings of capacitor voltage, $v_{Cf}$, and grid side inductor current, $i_{Lfg}$. The state-space equations for the discrete-time state estimator can be expressed in standard matrix format of

$$
\dot{X}_{k+1} = A_E \dot{X}_k + B_E u_k + L_E (Y_k - \hat{Y}_k) 
$$

(6.13a)

$$
\hat{Y}_{k+1} = C_E \dot{X}_k + D_E u_k
$$

(6.13b)

where the variables and matrices for Luenberger observer represent

$$
A_E = \begin{bmatrix}
0 & -\frac{1}{L_{fs}} & 0 \\
\frac{1}{C_f} & 0 & -\frac{1}{C_f} \\
0 & 0 & 0
\end{bmatrix}, B_E = \begin{bmatrix}
\frac{1}{L_{fs}} \\
0 \\
0
\end{bmatrix},
$$

(6.14a)

$$
C_E = \begin{bmatrix}
0 & 1 & 0 \\
0 & 0 & 1
\end{bmatrix}, D_E = \begin{bmatrix}
0 \\
0
\end{bmatrix},
$$

(6.14b)

$$
\dot{X}_k = \begin{bmatrix}
\dot{i}_{Lfs}(k) \\
\dot{v}_{Cf}(k) \\
\dot{i}_{Lfg}(k)
\end{bmatrix}, \hat{Y}_k = \begin{bmatrix}
\hat{v}_{Cf}(k) \\
\hat{i}_{Lfg}(k)
\end{bmatrix}.
$$

(6.14c)

$L_E$ is a 3×2 observer gain matrix that can be tuned to achieve minimal estimation errors. The diagram of the state estimator is shown in Fig. 6.10. The state observer minimizes the estimation error, $e(k)$, with a dynamic equation of

$$
e_{k+1} = (A_E - L_E C_E) e_k.
$$

(6.15)

The estimation gain can be derived by
\[
L_E^T = RM^{-1}
\]  
(6.16)

where \( R \) is composed of tuning factors and \( M \) is determined by solving the Sylvester equation

\[
A_E^T M - M \Lambda = C_E^T R
\]
(6.17)

in which \( \Lambda \) is a matrix with the desired eigenvalues.

6.2.4 Local Level Variable Frequency Control

For the local level per phase variable-frequency critical-soft-switching control, two control strategies are proposed including variable-continuous-frequency critical-soft-switching (VCF-CSS)
Figure 6.14: The relationship of PWM carriers and fundamental sampling signals for VDF-CSS.

and variable-discrete-frequency critical-soft-switching (VDF-CSS). Two frequency controllers are implemented to achieve critical soft switching operation for high efficiency with different types of frequency. The VCF-CSS derives a continuous switching frequency based on the critical soft switching boundary conditions and then directly implements the frequency value to the PWM with the help of state estimator to collect the switch side inductor current value. On the other hand, VDF-CSS discretizes the calculated switching frequency with multiple times of the sampling frequency for PWM which does not need the state estimator to derive an accurate switch side inductor current value. Fig. 6.11(a) and 6.11(b) show the switch side inductor current waveforms for VCF-CSS and VDF-CSS, respectively. The envelopes of VCF-CSS and VDF-CSS are smooth and discretized due to the varying types of switching frequency. Both methods can achieve critical soft switching operation for the improvement of efficiency. Since both the VCF-CSS and VDF-CSS are combined with MPC to deal with the time-varying switching frequency, the transient performance is improved by MPC with less oscillation and spikes even for the discretized frequency. And the corresponding $\frac{di}{dt}$ stress on the switches are low.

**VCF-CSS**

VCF-CSS is designed to calculate the desired continuous switching frequency based on the peak/valley switch side inductor current and the critical soft switching boundary conditions in equation (6.1). The control diagram of the per phase power module with VCF-CSS and MPC has
been shown in Fig. 6.12 which includes MPC controller, state estimator and VCF-CSS controller. For the VCF-CSS controller, the continuously varying switching frequency, $f_{s,cal}$, is derived based on the threshold current, $I_{th}$, of critical soft switching boundary conditions in (6.1). Since the switch side inductor current ripple, $\Delta i_{Lfs}$, can be calculated as

$$\Delta i_{Lfs} = \frac{d(1-d)v_{dc}}{f_sL_{fs}}, \quad (6.18)$$

And the critical soft switching boundary conditions require the peak/valley inductor current values to be higher than $I_{th}$ and lower than $-I_{th}$, respectively. Thus, the calculation of the continuously varying switching frequency, $f_{s,cal}$, can be expressed as

$$f_{s,cal} = \frac{(1-d)d v_{dc}}{2(i_{Lfs,ave} + I_{th})L_{fs}}, \quad i_{Lfs,ave} \geq 0 \quad (6.19a)$$

$$f_{s,cal} = \frac{(1-d)d v_{dc}}{2(I_{th} - i_{Lfs,ave})L_{fs}}, \quad i_{Lfs,ave} \leq 0 \quad (6.19b)$$

where $i_{Lfs,ave}$ is the average value of switch side inductor current without considering the high current ripple for critical soft switching calculation. The $i_{Lfs,ave}$ have also been plotted as the blue sine waveform lines in Fig. 6.11.

As is shown in Fig. 6.12, the VCF-CSS receives the estimated values of $i_{Lfs,est}$, $v_{Cf,est}$ and $i_{Lfg,est}$ from the state estimator and optimal duty cycle value from MPC controller to calculate the desired switching frequency, $f_{s,cal}$, and applies to the PWM. The state estimator contributes to providing a more accurate switch side inductor current value for frequency calculation compared with the direct sampling value since the sampling frequency and control frequency are both constant. The varying switching frequency could result in a deviation of sampling from the true averaged inductor current value especially when the current ripple is large for critical soft switching. This deviation error can be solved by the state estimator.
**VDF-CSS**

Another frequency controller is designed as VDF-CSS to further discretize the calculated switching frequency in equations (6.19). The local per phase power module control with VDF-CSS is shown in Fig. 6.13. The continuously varying switching frequency in equations (6.19) is further discretized into pre-defined frequency bandwidth sections which is designed as integral multiple of the fundamental sampling frequency, $f_{s,\text{base}}$. Thus, the discretized varying switching frequency for PWM signals could be $n$ times of $f_{s,\text{base}}$ ($n \in \mathbb{Z}$). To ensure the soft switching operation, the multiple value of $n$ is rounded down during the discretization by choosing a relatively lower switching frequency section. The implementation of the frequency controller is shown in the left bottom block of Fig. 6.13. The relationship of PWM switching carrier signals and sampling signals are shown in Fig. 6.14 with a varying switching frequency from $4f_{s,\text{base}}$ to $2f_{s,\text{base}}$ then to $f_{s,\text{base}}$. The process of frequency discretization can be expressed as

$$f_{s,\text{discrete}} = nf_{s,\text{base}} = \text{floor}\left(\frac{f_{s,\text{cal}}}{f_{s,\text{base}}}\right) f_{s,\text{base}}. \quad (6.20)$$

The discretized frequency may be ringing back and forth by the oscillation of sampling noise during frequency changing transients. A hysteresis loop is configured after the frequency discretization process to eliminate the frequency oscillation. Then, the discretized frequency will be implemented to the PWM for soft switching operation.

Compared with the VCF-CSS, the VDF-CSS discretizes the switching frequency to be multiple times of the fundamental sampling frequency. Thus, the switch side inductor current will be sampled exactly at the average points of the current ripple without deviation from the accurate values as is shown in Fig. 6.14. Thus, even without the state estimator for the estimation of $i_{L,fs}$, the inductor current sampling can be accurate for the critical soft switching calculation at high current ripple.
Figure 6.15: Hardware prototypes of (a) integrated prototype (b) power board (c) medium frequency inductor and (d) high frequency inductor.

Figure 6.16: Switching frequency of VCF-CSS and VDF-CSS for (a) medium frequency and (b) high frequency applications.
Figure 6.17: Captured experimental readings of sampling measurement in blue lines and estimation in red lines of (a) switch side inductor current (b) capacitor voltage and (c) grid side inductor current.

Figure 6.18: Captured experimental readings of switching frequency in blue lines and grid side inductor current in red lines of (a) VCF-CSS and (b) VDF-CSS at medium frequency of 40kHz-240kHz with 45µH switch side inductor.
Figure 6.19: Captured experimental readings of switching frequency in blue lines and grid side inductor current in red lines of (a) VCF-CSS and (b) VDF-CSS at high frequency of 360kHz-1.08MHz with 4.5\(\mu\)H switch side inductor.

Figure 6.20: (a) The inductor current, capacitor voltage, grid current and DC bus voltage with constant switching frequency and (b) zoomed waveforms.

6.3 Results

The proposed variable-frequency critical-soft-switching model predictive control methods with state estimator for zero-sequence stabilized non-isolated grid-connected inverter have been vali-
Figure 6.21: Medium frequency of 40kHz-240kHz with 45\(\mu\)H switch side inductor (a) VCF-CSS and (b) zoomed steady state waveforms of inductor current, capacitor voltage, grid current and DC bus voltage.

Figure 6.22: High frequency of 360kHz-1.08MHz with 4.5\(\mu\)H switch side inductor (a) VCF-CSS and (b) zoomed steady state waveforms of inductor current, capacitor voltage, grid current and DC bus voltage.

dated experimentally with carefully designed litz wire inductors and power converter board. The control strategies and modified topology are applied to both medium frequency of 40kHz-240kHz with 45\(\mu\)H switch side inductor and high frequency of 360kHz-1.08MHz with 4.5\(\mu\)H switch side inductor, respectively. The maximum efficiency at rated power of 15kW is reaching 99%. The
Figure 6.23: Medium frequency of 40kHz-160kHz with 45\(\mu\)H switch side inductor (a) VDF-CSS and (b) zoomed steady state waveforms of inductor current, capacitor voltage, grid current and DC bus voltage.

Figure 6.24: High frequency of 360kHz-1.08MHz with 4.5\(\mu\)H switch side inductor (a) VDF-CSS and (b) zoomed steady state waveforms of inductor current, capacitor voltage, grid current and DC bus voltage.

Power densities of 8.14kW/L and 10.4kW/L are achieved for medium and high frequencies, respectively. The detailed performances of the proposed control methods on the modified non-isolated inverter are shown as follows.
Figure 6.25: The drain-source voltage and current across the upper switch for soft switching operation.

Figure 6.26: (a) VCF-CSS and (b) zoomed transient waveforms of inductor current, capacitor voltage and DC bus voltage with a current step of 4A.

Figure 6.27: (a) VDF-CSS and (b) zoomed transient waveforms of inductor current, capacitor voltage and DC bus voltage with a current step of 4A.
Figure 6.28: The efficiency curves comparison of VCF-CSS, VDF-CSS and constant frequency.

Figure 6.29: The loss comparison between the conventional $LCL$ inverter and the developed inverter with VF-CSS.

6.3.1 Hardware Setup

The testbench is shown in Fig. 6.15 including the power converter board in Fig. 6.15(b) and switch side medium inductor in Fig. 6.15(c) and small inductor in Fig. 6.15(d). The DSP control card, TMS320F28388D, is plugged on side of the power converter board. The Cree SiC MOSFET,
Figure 6.30: The (a) power-frequency and (b) efficiency-power density diagrams of SiC and GaN based applications.

C3M0032120K, is chosen for the power switch in the middle area of the power board covered by the heat sink and cooling fan. For the switch side $LCL$ inductors, two types of inductors with $45\mu H$ and $4.5\mu H$ are designed at rated power for the medium frequency of $40kHz-240kHz$ and high frequency of $360kHz-1.08MHz$ operations, respectively. The switching frequency as functions of output power for high/medium frequencies VCF-CSS/VDF-CSS are also shown in Fig. 6.16. The dead time is configured as 80ns for the safety consideration. Thus, the maximal modulation indexes for the medium and high frequency inductor applications are calculated as 0.98 for 240kHz and 0.91 for 1.08MHz, respectively.

For the medium inductor in Fig. 6.15(c), air-gaped E-E core is designed with E42/21/20-3F3 from Ferroxcube to be combined with litz wire winding (equivalent gauge 10). For the small inductor in Fig. 6.15(d), air-gaped E-I core is designed with E42/21/20-3F3 from Ferroxcube to be combined with litz PCB winding for the purpose of saving window space to reduce the inductor volume as has been designed in [133].

For the output capacitors, each phase has three $2.5\mu F$ upper caps and three $2.5\mu F$ lower caps.
in parallel all from TDK FA10 to be integrated on the power board. The grid side inductor is composed of two 1μH in series for each each phase on the board.

For the parameters design of output capacitance and grid side inductance, the principles are based on the minimum output capacitor voltage ripple, $v_{Cf,ripple}$ and the resonant frequency of the $LCL$ filter, $\omega_{res}$. Specifically, the minimum capacitance is determined by the output voltage ripple which is expressed as:

$$C_{f,min} = \frac{1 - d_{min}}{8L_{fs}v_{Cf,ripple}[\%]f_{sw}^2}. \quad (6.21)$$

Then, from the minimum available $C_{f,min}$, the value of grid inductance can be adjusted to determine the resonant frequency of $LCL$ filter system as is shown in

$$\omega_{res} = \sqrt{\frac{L_{fs} + L_{fg}}{L_{fs}L_{fg}C_{f}}}. \quad (6.22)$$

6.3.2 State Estimation Results

The state estimation method is validated in the modified non-isolated $LCL$ grid-connected inverter to be combined with the VCF-CSS and MPC. One purpose of the estimator is to provide accurate switch side inductor current readings, $i_{Lfs}$, for both the calculation of optimal soft switching frequency and MPC implementation with fixed control frequency at high current ripple. Another purpose is to reduce the sampling noise from the sensors for a better steady state performance.

The observer estimates the switch side inductor current, $\hat{i}_{Lfs}$, capacitor voltage, $\hat{v}_{Cf}$, and grid side inductor current, $\hat{i}_{Lfg}$, with the ADC measurements of capacitor voltage, $v_{Cf}$, and grid side inductor current, $i_{Lfg}$. Fig. 6.17 shows the experimental readings from DSP of the estimated $\hat{i}_{Lfs}$, $\hat{v}_{Cf}$, $\hat{i}_{Lfg}$ in blue lines and the measured $i_{Lfs}$, $v_{Cf}$, $i_{Lfg}$ in red lines. The observer accurately estimates the measurements of $LCL$ system. And the sampling noises from the measurements are reduced with observer to provide cleaner and smoother current/voltage information for VCF-CSS and MPC.
6.3.3 Steady State Results

The steady state experimental results of VCF-CSS and VDF-CSS with MPC and estimator are shown in this section to demonstrate the critical soft switching performance for both medium frequency (40kHz-240kHz, 45\(\mu\)H) and high frequency (360kHz-1.08MHz, 4.5\(\mu\)H) testing setups.

Fig. 6.18 shows the captured data of switching frequency and the corresponding AC current with medium frequency ranged at 40kHz-240kHz on the 45\(\mu\)H inductor test bench. Specifically, Fig. 6.18(a) captures the VCF-CSS data of switching frequency and AC current based on the control method in Fig. 6.12 and equation (6.19). Fig. 6.18(b) captures the VDF-CSS data of switching frequency and AC current based on the control method in Fig. 6.13. The variable discrete frequency is separated into three discretized levels including 40kHz, 80kHz and 160kHz which are all multiple times of the fixed sampling frequency of 40kHz. Thus, the switch side inductor current can be sampled more accurately at high current ripple even without estimation.

Fig. 6.19 shows the captured data of switching frequency and the corresponding AC current with high frequency ranged at 360kHz-1.08MHz on the 4.5\(\mu\)H inductor test bench. Specifically, Fig. 6.19(a) captures the VCF-CSS data of switching frequency and AC current based on the control method in Fig. 6.12 and equation (6.19). Fig. 6.19(b) captures the VDF-CSS data of switching frequency and AC current based on the control method in Fig. 6.13. The variable discrete frequency is separated into four discretized levels including 360kHz, 600kHz, 840kHz and 1.08MHz which are all multiple times of the fixed sampling frequency of 120kHz. Thus, the switch side inductor current can be sampled more accurately at high current ripple even without estimation.

The experimental waveforms of switch side inductor current, capacitor voltage, grid current and DC voltage are compared between the hard switching and the proposed VCF-CSS and VDF-CSS in Fig. 6.20 to Fig. 6.24. Specifically, in Fig. 6.20, a fixed switching frequency of 80kHz is implemented which results in hard switching at the peak and valley points of the sinusoidal AC current waveforms. Fig. 6.21 and Fig. 6.22 show the VCF-CSS and zoomed waveforms at medium and high frequency, respectively. The critical soft switching operations are maintained at the full
AC current period. Fig. 6.23 and Fig. 6.24 show the VDF-CSS and zoomed waveforms at medium and high frequency, respectively. The critical soft switching operations can also be maintained by the discretized frequency at the full AC current period. Since the main target of VF-CSS is to achieve soft-switching turn-on of the upper switch, the detailed drain-source voltage and current waveforms across the upper switch for soft switching are shown in Fig. 6.25 to illustrate the ZVS operation.

6.3.4 Model Predictive Control Transient Results

The transient experimental results for the proposed MPC controller with state estimator are shown in this section to demonstrate the improved dynamic performance of the proposed MPC for the variable frequency operation and during current reference steps.

The transient experimental results and the zoomed waveforms for VCF-CSS-MPC and VDF-CSS-MPC are shown in Fig. 6.26 and Fig. 6.27 with a current step of 4A, respectively. From the zoomed switch side inductor current waveforms, the critical soft switching operations are fully maintained during both the current step transients and switching frequency transition instants.

6.3.5 Efficiency and Power Density Results

The efficiencies of the proposed VCF-CSS and VDF-CSS control strategies have been tested up to the rated power as is shown in Fig. 6.28. The efficiencies of above 99% are both achieved for the VCF-CSS and VDC-CSS which are 2% higher than the hard switching operation. Also the loss breakdown comparison between the developed inverter with VF-CSS and the conventional \( LCL \) inverter with hard switching is shown in Fig. 6.29. With the proposed method, the switching loss is reduced by more than times. And with the high frequency inductor and power board design in Fig. 6.15, a maximum power density of 10.4kW/L is achieved. Several typical SiC/GaN converter designs are compared in Fig. 6.30 with the power-frequency and efficiency-power density plots [134, 135, 136, 137, 138, 139, 140, 141, 142, 143]. The proposed design is labeled in red star and achieves the Pareto Optimal Points.
6.4 Summary

This chapter proposes variable-frequency critical-soft-switching model predictive control strategies to improve the efficiency and power density of a modified non-isolated grid-connected inverter. Also, a state estimator is developed to be combined with the variable frequency model predictive controller for the improvements of sampling accuracy and noise rejection. The leakage current is attenuated by the zero-sequence model predictive control and the modified non-isolated topology. Two types of variable frequency controllers are developed including VCF-CSS and VDF-CSS to achieve the critical soft switching operation. A Luenberger Observer is developed to be combined with the VCF-CSS for more accurate inductor current calculation of critical soft switching and noise rejection. The proposed control methods and modified non-isolated topology have been validated on medium frequency (>200kHz, 45μH) and high frequency (>1MHz, 4.5μH) test benches, respectively. With the proposed critical soft switching control strategies, the efficiency is above 99% at the rated power of 15kW and a power density of more than 10.4kW/L is achieved.
Chapter 7: Design Case of MPC-Based Regulated Third Harmonic Injection for Zero-Sequence Stabilized $LCL$ Inverter

In the grid-connected power converter applications such as electric vehicle (EV) charger and photovoltaic (PV), leakage current issue and DC bus utilization are two key factors that influence the performance. For the leakage current issue, a bulky line frequency transformer is typically installed to block the leakage path at the point of common coupling (PCC) which increases the cost, volume and weight of the system. For the DC bus utilization, the DC bus voltage needs to be stepped up to be at least twice of the grid voltage amplitude to avoid saturation issue which brings extra switching losses and challenges to the switch voltage tolerance capability. This chapter focuses on the combination of modular MPC with zero-sequence voltage control and regulated third harmonic injection (THI) techniques in the modified non-isolated three-phase $LCL$ converter. The developed software-defined power electronics architecture in Chapter 5 is leveraged to implement the MPC-based regulated third harmonic injection technique.

For the DC bus utilization of DC/AC inverters, the THI can be implemented to avoid duty cycle saturation with a relatively low DC voltage [144]. To evaluate the DC bus utilization, a modulation index can be calculated as the ratio of AC output voltage fundamental component (grid voltage) peak value to the modulation waveform fundamental component (DC bus voltage) peak value. Several methods have been studied to improve the DC bus utilization, e.g., third harmonic sinusoidal waveform injection for sinusoidal PWM (SPWM), triangular waveform injection for space vector pulse width modulation (SVPWM) [145]. Among the aforementioned injection methods, the SPWM-based mechanism is simpler to implement in the DSP [146], [147]. However, if the third harmonic or triangular waveforms are directly injected in the duty cycle before the modulation, the control stability and robustness will be affected and even the divergence could occur in the
PWM modulation. Also, the conventional THI approaches will inject extra harmonics to the grid which will deteriorate the power quality of the grid voltage and current. Even [146] and [147] have proposed optimized THI algorithms to minimize the grid distortion of THI, the injected grid harmonics cannot be fully eliminated. And the optimization look-up table from the published methods accounts for extra computation resources and brings more control complexity. For the modulation contribution of this chapter, a simple MPC-based zero-sequence regulated third harmonic injection method is proposed without the need of introducing optimization algorithm and no extra harmonics are injected to the grid. The power quality and system stability are improved. Combined with the proposed topology and MPC-based regulated THI method, the DC bus utilization is improved in a robust way without injecting harmonics to the grid and the complexity of optimization methods in [146] and [147] are saved.

This chapter is organized as follows. Firstly, the circuitry model of the proposed non-isolated three-phase grid-connected converter in Fig. 7.1(b) is analyzed in detail. Compared with the conventional topology in Fig. 7.1(a), the common points of the output capacitors are connected to the positive/negative terminals of the DC bus to bypass the leakage current and stabilize the common mode voltage. The common mode circuit with parasitic path is illustrated. Also the equivalent circuit model in dq0 reference frame is analyzed. Secondly, the proposed modular MPC control method is introduced with zero-sequence voltage controller to stabilize the common mode voltage. The control mechanism includes the central level grid current dq control and local level MPC of zero-sequence voltage control and three-phase capacitor voltage/inductor current control. The local MPC module algorithm is designed based on the management of switch side per phase LC filter inductor current and capacitor voltage. An explicit MPC method is applied for local module to save the execution time. Thirdly, the regulated third harmonic injection method is proposed based on the zero-sequence voltage control to improve the DC bus voltage utilization without injecting extra harmonics to the grid. The advantages of the proposed methods can be concluded as non-isolated zero-sequence voltage MPC for common mode improvement, per phase explicit modular MPC for reducing DSP calculation complexity, regulated THI based on zero-sequence voltage control for
a stable and robust implementation of DC bus utilization improvement without extra harmonics to deteriorate the grid and the inner loop MPC for transiente performance improvement. No grid side inductance value is needed for the two-layer cascaded control structure which both improves the dynamic performance from inner MPC loop and avoids the MPC parametric error caused by the uncertainty of grid side inductance. Also, the modular concept of local MPC module enables the extensibility for the power converter control with a flexible number of phases. Finally, the experimental results are shown to validate the proposed control methods.

7.1 System Modeling

The leveraged non-isolated three-phase DC/AC converter has been shown in Fig. 7.1(b). Different from the traditional two-level three-phase DC/AC converter, the common point of three-phase capacitors is connected to the DC bus positive/negative terminals to create a bypassing path for zero-sequence voltage model predictive control. By leveraging the topological modification and zero voltage control, the common mode voltage can be stabilized to reduce the leakage current.

7.1.1 DC/AC LCL Converter Modeling

The DC/AC converter is directly interfaced with the grid. To maintain a constant common mode voltage, the proposed control method is based on the $dq0$ coordinate system to leverage the zero-sequence voltage component in the proposed topology. Compared with the $abc$ system, the
active/reactive power and common mode voltage can be controlled independently with d, q and 0 sequence components in a dq0 system. The coordinate system model of the proposed DC/AC converter can be derived from abc reference frame.

**abc system**

The state space equations in abc system are expressed as:

\[
\begin{align*}
\dot{i}_{L,abc} &= \frac{1}{L_{fs}} I_{L,abc} - \frac{1}{L_{fs}} I_{u,c,abc} \\
\dot{u}_{c,abc} &= \frac{1}{C_f} I_{L,abc} - \frac{1}{C_f} I_{g,abc} \\
\dot{i}_{g,abc} &= \frac{1}{L_{fg}} I_{u,c,abc} - \frac{1}{L_{fg}} I_{u,g,abc},
\end{align*}
\]

(7.1a) (7.1b) (7.1c)

where \(L_{fs}, C_f\) and \(L_{fg}\) are the switch side inductor, capacitor and grid side inductor, respectively, for the LCL filter. \(i_{L,abc}, u_{c,abc}, i_{g,abc}\) and \(u_{x,abc}\) are the switch side inductor current, capacitor voltage, grid side current and grid voltage, respectively. \(I \in \mathbb{R}^{3 \times 3}\) is the identity matrix.

**dq0 system**

Since it is difficult to control the time-varying sinusoidal references in abc system while convenient to calculate the active/reactive power and stabilize zero-sequence voltage in dq0 system, the state space model is transformed to dq0 reference frame for control purpose of the proposed method. Coordinate system transformation has been widely applied in the three-phase AC systems because the dq system can transfer the time-varying sinusoidal waveforms to equivalent constant DC values [148]. For the implementation of control, the DC values are much easier to be controlled than AC values. However, the traditional methods mainly utilize the \(dq\) system without considering the zero-sequence. The proposed topology connects the common point of AC three-phase capacitors to the DC bus positive/negative terminals which permits to extract the zero-sequence from abc system to dq0 system and control the zero-sequence voltage to be half of DC bus voltage. Thus,
the \( u_{cm} \) can be stabilized accordingly.

For the reference frame transformation with zero-sequence components, \( abc \) system needs to be firstly transformed to \( \alpha\beta0 \) and then to \( dq0 \) system. From \( abc \) to \( \alpha\beta0 \), the Clarke transform is applied as:

\[
x_{\alpha\beta0} = \mathbf{T} x_{abc} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} x_{abc}.
\] (7.2)

In \( \alpha\beta0 \) system, the signals are composed of two orthogonal sinusoidal AC waveforms in \( \alpha \) and \( \beta \) frames and a zero-sequence component. A Park transform is implemented secondly to convert the stationary reference frame of \( \alpha\beta0 \) to the rotating \( dq0 \) system which is calculated as:

\[
x_{dq0} = \mathbf{P}(\theta) x_{\alpha\beta0} = \begin{bmatrix} \cos \theta & \sin \theta & 0 \\ -\sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix} x_{\alpha\beta0}.
\] (7.3)

\( \theta \) is the phase angle of the grid which is tracked with a phase-locked-loop (PLL) controller by measuring the grid voltage at the point of common coupling (PCC). Thus, the AC sinusoidal signals in \( abc \) are converted to DC values in a rotating \( dq0 \) frame with a time-varying angle of \( \theta \). Considering the control requirements to finally implement the duty cycles in \( abc \) format for the PWM modulation, the inverse Clarke and Park transformations are needed to convert the output of control signals from \( dq0 \) to \( abc \):

\[
x_{abc} = \mathbf{T}^{-1} x_{\alpha\beta0} = \mathbf{T}^{-1} \mathbf{P}(\theta)^{-1} x_{dq0}.
\] (7.4)

Based on equations (7.2) and (7.3) of the coordinate system transformations, the state space equations of (7.1) can be transformed from \( abc \) to \( dq0 \):
\[ i_{L,dq0} = \frac{1}{L_{fs}} i_{u,x,dq0} - \frac{1}{L_{fs}} i_{u,c,dq0} - \omega G i_{L,dq0} \]  \hspace{1cm} (7.5a)

\[ \dot{u}_{c,dq0} = \frac{1}{C_f} \dot{I}_{L,dq0} - \frac{1}{C_f} \dot{I}_{g,dq0} - \omega G u_{c,dq0} \]  \hspace{1cm} (7.5b)

\[ \dot{i}_{g,dq0} = \frac{1}{L_{fg}} i_{u,c,dq0} - \frac{1}{L_{fg}} i_{u,g,dq0} - \omega G i_{g,dq0} \]  \hspace{1cm} (7.5c)

where \( \omega \) is the angular velocity of the grid in rad/s. \( G \) is the matrix for the coupling terms resulted from the transformation:

\[
G = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}.
\]  \hspace{1cm} (7.6)

By leveraging the \( dq0 \) state space equations and the connection of three-phase capacitors common point with DC bus positive/negative terminals, the zero-sequence voltage can be controlled explicitly to stabilize the \( u_{cm} \).

The equivalent circuits of the \( dq0 \) system for proposed topology of DC/AC side converter are shown in Fig. 7.2.

### 7.1.2 Common Mode Modeling

For a conventional transformerless three-phase grid-connected system as is shown in Fig. 7.1(a), there exist common mode leakage current paths among the grid neutral, chassis of the power module and DC ground due to the high frequency common mode voltage, \( v_{cm} \), fluctuation on the switch side and the equivalent parasitic capacitance, \( C_p \) [149]. The leakage current, \( i_{lkg} \), will flow through the common mode path and can be derived as:

\[ i_{lkg} = C_p \frac{d v_{cm}}{dt} \]  \hspace{1cm} (7.7)
Figure 7.2: (a) $d$-axis (b) $q$-axis and (c) 0-axis equivalent circuit of the modified topology on DC/AC side.

Figure 7.3: Equivalent common mode circuit of the (a) conventional and (b) proposed non-isolated DC/AC converter.

The level of leakage current is mainly dominated by the fluctuating rate of common mode voltage and equivalent impedance of parasitic capacitance [150], [151]. The fluctuation of common mode voltage is induced by the intrinsic high switching frequency of the circuit and can be expressed as the mean value of three-phase switching legs output voltages, $v_{x,a}, v_{x,b}, v_{x,c}$:

$$v_{cm} = \frac{v_{x,a} + v_{x,b} + v_{x,c}}{3}. \quad (7.8)$$
Fig. 7.3(a) shows the equivalent common mode circuit in a traditional non-isolated DC/AC converter where the red dotted lines with arrows represent the leakage current. This leakage current is excited by the high frequency fluctuation of common mode voltage in the parasitic path. So, the leakage current is mainly determined by two factors: (1) rate of $u_{cm}$; (2) parasitic capacitance. Firstly, according to equation (7.8), the mean value of three-phase switching legs output voltages is square waveforms with an amplitude of DC bus voltage at switching frequency level. Thus, the rate of change, $du_{cm}/dt$ is high to amplify the leakage current. Secondly, the parasitic capacitance, $C_p$ is another factor to influence the leakage current. The value of $C_p$ varies in the solar and EV charging systems. For a typical photovoltaic system, $C_p$ is ranged between 10nF-100nF. However, in an EV system, $C_p$ is between 1nF-10nF [152]. For the safety consideration of the standard requirements, the leakage current is limited to be no more than 30mA in an EV system by IEC 62955:2018 and IET Wiring Regulation 18th Edition (BS 7671:2018) Section 722.531.2.101.

Fig. 7.3(b) presents the equivalent common mode circuit in the proposed non-isolated DC/AC converter where the leakage current to the grid can be bypassed with the connection of three-phase output capacitors common point and DC positive/negative terminals. This leakage current attenuation capability is achieved by the proposed zero-sequence voltage controller which aims at stabilizing the zero-sequence capacitor voltage to be a constant value of half DC bus voltage, $u_{dc}/2$, instead of a high frequency fluctuating square waveform.
7.2 Control Design

The proposed model predictive control method of non-isolated three-phase $LCL$ converter with zero-sequence voltage stabilization capability is illustrated in this section. Fig. 7.4 shows the control diagram which consists of the central level control of $dq$ sequences output current PI control cascaded with the local level control of zero-sequence voltage, three-phase inductor current/capacitor voltage model predictive control. The local level modular MPC is implemented for each phase of LC module. The modularized local MPC enables the extensibility for random phase number of power converter control and reduces the computational complexity of multi-phase MPC algorithm as a whole function.

7.2.1 Phase-locked-loop

The transformations between $abc$ and $dq0$ needs the real-time phase angle information, $\theta$, of the grid voltage [153]. An effective way can be implemented with a PI controller by controlling the $q$ component of the grid voltage, $v_{g,q}$, to be zero to derive the angular velocity, $\omega$, of the phase angle. Then, the $\theta$ can be calculated with a period of $2\pi$. And based on the active/reactive power calculation in

$$\begin{bmatrix}
P \\
Q
\end{bmatrix} = \frac{3}{2} \begin{bmatrix}
u_{g,d} & u_{g,q} \\
u_{g,q} & -u_{g,d}
\end{bmatrix} \begin{bmatrix}
i_{g,d} \\
i_{g,q}
\end{bmatrix}$$

(7.9)

the $d$-axis and $q$-axis represent the active and reactive power, respectively.

7.2.2 Central Level Output Current Control

The output current is transformed from $abc$ to $dq$ reference frame with Clarke and Park transformations. Then, two PI controllers are configured to regulate the $dq$ sequence output currents, $i_{g,d}$ and $i_{g,q}$, respectively. Based on the configuration of PLL to control the $q$ component of grid voltage, $v_{g,q}$, to be zero and the active/reactive equation in (7.9), $i_{g,d}$ and $i_{g,q}$ are linked to the
active and reactive power control loops, respectively. The outputs of grid current controller are the references of $dq$ sequence capacitor voltages, $v_d^*$ and $v_q^*$, which will be transformed back to $abc$ reference frame and configured as the MPC reference of three-phase capacitor voltages.

7.2.3 Zero-sequence Voltage Control

The zero-sequence voltage of the three-phase capacitors are controlled to be half of DC bus voltage with MPC to block the leakage current from flowing through the grid. As are shown in Fig. 7.2(c) of the 0-axis equivalent circuit and Fig. 7.3(b) of the $abc$ frame equivalent common mode circuit, the zero-sequence output current can be attenuated by the stabilization control of zero-sequence capacitor voltage. Specifically, half of DC bus voltage measurement is configured as the reference of zero-sequence voltage controller and transformed from $dq0$ to $abc$ frame for the three-phase LC capacitor voltage model predictive control. A third harmonic component extracted from the central level grid side inductor current controller output after reversed Park transformation can be added to the zero-sequence voltage reference to improve the DC bus voltage utilization which will be analyzed in the fourth section.

The working principle of zero sequence voltage control is based on the three phase output capacitor voltage reference MPC tracking. Specifically, in the central controller, the zero sequence component of the reference is designed as half of DC bus voltage measurement, $V_{dc}/2$. This reference is combined with $dq$ components references from the output of grid side inductor current controllers and then transformed into $abc$ reference frame for tracking references of the local three phase MPC controllers. Each of the reference input for three phase local MPC controller is composed of a sinusoidal AC component and a zero sequence DC component. Thus, the object and cost function of the zero sequence voltage MPC control is integrated into the three separate MPC configurations which is consistent with the illustration in (6.7). The three phase local MPC tracking for zero sequence voltage control guarantees a stabilized common mode capacitor voltage and low leakage current.
7.2.4 Local Level Per Phase LC Filter MPC

The explicit MPC method is designed for the switch side capacitor voltage and inductor current control by following the local level per phase MPC algorithms in Chapter 6 from (6.3) to (6.12). As is shown in Fig. 7.4 of the control diagram, the three-phase capacitor voltages are controlled in $abc$ frame to follow the references from the cascaded grid current controller’s outputs. The switch side inductor currents are also regulated with the MPC by adjusting the weighting factor between $i_{L,abc}$ and $u_{c,abc}$.

For the MPC implementation, in every control period, the MPC controller receives the measured switch side inductor current, $i_{L,abc}$, capacitor voltage, $v_{c,abc}$, grid current, $i_{g,abc}$, from ADC and capacitor voltage reference, $v^*_{c,abc}$ from the grid current controller. An offline generated piecewise affine search tree is applied to derive the optimal duty cycle for the explicit MPC.

7.2.5 Modular MPC Concept Based on Software-Defined Architecture

The proposed regulated THI control structure is designed based on the software-defined power electronics architecture in Fig. 5.1. The whole control structure is composed of central control layer and local level MPC control modules. The central controller is functioned as a pivot to collect the ADC data from local modules, manage the converged branch power control, redistribute the power flow for local modules and generate voltage/current references for local modules. The local module focuses on the MPC control, ADC sampling and PWM modulation of LC filtered switch leg. Thus, the reference commands are allocated to the local control modules and the ADC data are collected for the local and central controllers. The modular MPC concept enables a more general power converter control with random number of power modules to satisfy the topological and power rating requirements. To satisfy different topological requirements, the local MPC can be applied to single/three phase DC/AC or DC/DC converters. Also, the number of paralleled modules is adjustable with central controller to redistribute the power flow for local modules to meet different power rating demands.

The comparative analysis of the proposed modular MPC and the conventional methods can be
concluded as: (1) Firstly, the grid side inductor current is controlled with PI while the output capacitor voltage and switch side inductor current are controlled with MPC. No grid side inductance value is needed for the two-layer cascaded control structure which both improves the dynamic performance from inner MPC loop and avoids the MPC parametric error caused by the uncertainty of grid side inductance. (2) Secondly, the proposed MPC is operated in a modular way for each phase $L_C$ filter with simpler state space matrix formulation and smaller size of C code for experimental implementation in DSP. The state space matrix of $A$ is $2\times2$ which is smaller than $4\times4$ in [109] and $6\times6$ in [126]. The generated C code file for MPC implementation is only 5kB which is undemanding for a less costly DSP; (3) Thirdly, the proposed local MPC controllers and central controller can be implemented in different interrupts, cores or digital control devices with different frequencies. CAN protocols can be leveraged to communicate among the controllers. The local MPC controllers are configured with higher frequencies than the central controller. This implementation is designed to enable a higher control bandwidth for the local MPC than the central controller to improve the dynamic performance. Due to the simplified C code file of the proposed MPC controller, the execution time of each MPC algorithm is within 5us. Thus, the local MPC can be implemented with a frequency of 40kHz while the central controller is operating at 20kHz; (4) Finally, the local MPC controllers are implemented in $abc$ reference frame for the switch side $LC$ filter components. And the grid side inductor current is manipulated by the central level grid current controller. Thus, as is shown in equation (6.5a), the state space matrices are only composed of the static parameters of switch side inductance, $L_{fs}$, output capacitance, $C_f$, and control period, $T_s$. Different from the formulations of state space matrices in [109] and [126], no dynamic parameter, such as the grid angular velocity $\omega$, is included in the state space matrices. A PLL controller is designed to provide the accurate grid angular velocity. All static parameters for the state space matrices guarantee an offline generated explicit MPC function which saves the execution time for the online operation of MPC algorithm.
Figure 7.5: (a) Conventional (b) proposed regulated third harmonic injection methods and (c) the detailed control diagram of the zero sequence stabilized RTHI.

Figure 7.6: (a) Sinusoidal THI and (b) Triangular space vector injection.
7.3 Regulated Third Harmonic Injection

A regulated third harmonic voltage injection (RTHI) method is proposed in this chapter based on the zero voltage MPC to improve the DC bus voltage utilization. Different from the conventional THI (Con-THI) in Fig. 7.5(a) to directly apply the third order sinusoidal waveform or triangular space vector component to the duty cycle for modulation, the proposed RTHI in Fig. 7.5(b) extracts the third order/triangular components from the central level grid side inductor current controller output after reversed Park transformation and add them to the zero-sequence voltage reference, $v_{dc}/2$, to formulate a new third-harmonic-based zero-sequence reference for the MPC. The main advantages of the proposed RTHI include: (1) As is shown in Fig. 7.4, the injection of third order/triangular components will be regulated by the MPC constraints before applying to the duty cycle of PWM. Thus, compared to the traditional direct duty cycle side injection methods, the stability and robustness of the system are improved. (2) By leveraging the proposed modified $LCL$ converter to connect the capacitors common point to positive/negative DC bus in Fig. 7.1(b), the injected third harmonic components will be bypassed by the modified paths without flowing into the grid. Thus, the grid-connected power quality will be improved compared to the conventional THI methods. The third order sinusoidal (Sin-RTHI) and triangular space vector (Tri-RTHI) components injection methods are analyzed in this section.

7.3.1 Third Harmonic Sinusoidal Injection (Sin-RTHI)

The sinusoidal injection method is implemented by deriving the third order of grid fundamental frequency component to be superimposed to the zero-sequence voltage reference of MPC. The Sin-RTHI zero-sequence voltage reference for MPC can be expressed as:

$$v_{0,3rd}^* = v_{dc}/2 + V_m D_{3rd} \sin(3\omega t).$$

(7.10)

Thus, the $abc$ frame Sin-RTHI three-phase capacitor voltage references, $v_{c,abc}^*$, distributed to the local MPC controllers can be expressed as
\[ v_{c,a}^* = v_{c,a}^* + V_m D_{3rd} \sin(3\omega t) \quad (7.11a) \]
\[ v_{c,b}^* = v_{c,b}^* + V_m D_{3rd} \sin(3(\omega t - \frac{2\pi}{3})) \quad (7.11b) \]
\[ v_{c,c}^* = v_{c,c}^* + V_m D_{3rd} \sin(3(\omega t + \frac{2\pi}{3})). \quad (7.11c) \]

where \( V_m \) and \( D_{3rd} \) are the amplitude of fundamental component and third harmonic injection depth, respectively. The angular speed, \( \omega \), and phase shift can be derived based on the PLL controller. By leveraging the THI to the proposed zero-sequence voltage MPC as is shown in Fig. 7.5(b), the peak to peak capacitor voltage can be reduced to improve the DC bus utilization and avoid the duty cycle saturation in lower DC bus voltage. Fig. 7.6(a) shows the simulation waveforms of third order, fundamental frequency and injected capacitor voltages in one grid period.

### 7.3.2 Triangular Space Vector Injection (Tri-RTHI)

The triangular space vector injection method is implemented by deriving the mean value of maximum and minimum grid fundamental frequency component capacitor voltage to be superimposed to the zero-sequence voltage reference of MPC. The Tri-RTHI zero-sequence voltage reference for MPC can be expressed as:

\[ v_{0,3rd}^* = \frac{v_{dc}}{2} - D_{3rd} \left[ \max(v_{c,abc}^*) + \min(v_{c,abc}^*) \right]. \quad (7.12) \]

Thus, the \( abc \) frame Tri-RTHI three-phase capacitor voltage references, \( v_{c,abc}^* \), distributed to the local MPC controllers can be expressed as
\( v_{c,a}^* = v_{c,a}^* - D_{3rd}[\max(v_{c,abc}^*) + \min(v_{c,abc}^*)] \)  
(7.13a)

\( v_{c,b}^* = v_{c,b}^* - D_{3rd}[\max(v_{c,abc}^*) + \min(v_{c,abc}^*)] \)  
(7.13b)

\( v_{c,c}^* = v_{c,c}^* - D_{3rd}[\max(v_{c,abc}^*) + \min(v_{c,abc}^*)] \).  
(7.13c)

As is shown in Fig. 7.6(b) of the triangular component injection, the DC bus utilization can also be improved to avoid the duty cycle saturation issue.

To evaluate the effectiveness of the THI in Fig. 7.5, a voltage gain can be defined as the ratio of the fundamental component capacitor voltage peak value, \( v_{base} \), to the reference modulation waveform peak value, \( v_{THI} \).

\[
G_v = \frac{v_{base}}{v_{THI}}.  
\]  
(7.14)

The maximum voltage gain of the continuous THI methods can be derived at the \( \pi/3 \) when the third harmonic is at zero crossing point. Thus,

\[
G_{v,\text{max}} = \frac{1}{\sin(\pi/3)} \approx 1.155.  
\]  
(7.15)

By leveraging the proposed THI methods, the DC bus voltage can be reduced by a factor of 1.15 and the voltage stress, switching losses on the power switches can be decreased, accordingly.

### 7.3.3 Advantages of Zero-sequence Controlled RTHI

The advantages of the zero-sequence controlled RTHI are addressed in this subsection. The detailed working principle of the zero-sequence controlled RTHI is shown in Fig. 7.5(c). Different from the conventional THI in Fig. 7.5(a), the proposed RTHI methods extract the third order/triangular components from the central level grid side inductor current controller output after reversed Park transformation and superpose the third order/triangular components, \( v_{3rd}^* \), with
the zero sequence voltage reference, $v_{dc}/2$, as the new zero sequence reference for the local MPC to track. However, the conventional THI methods directly add the third order components onto the duty cycle for PWM modulation which brings two drawbacks: (1) The directly added third order components are from the output of PI controllers. No constraints and regulations are implemented before the third order components are pushed to the PWM modulation. Thus, compared to conventional THI, the proposed zero sequence stabilized RTHI is more robust and stable from the control perspective; (2) The conventional THI induces extra third harmonics to the grid with the traditional inverter topology which could deteriorate the power quality at PCC. The proposed zero sequence controlled RTHI combined with the proposed topology can bypass the third harmonics without injecting harmonics to the grid. The power quality will be improved automatically without extra optimization methods in [146] and [147] to reduce the THD at PCC.

7.4 Results

The proposed method is validated experimentally on the non-isolated three-phase converter with grid simulator. The testing parameters are 450Vdc to 208Vac with switching frequency
Figure 7.8: (a) Triangular RTHI and (b) zoomed waveforms.

Figure 7.9: (a) The transients from sinusoidal RTHI to constant zero-sequence voltage control and (b) zoomed waveforms.

of 100kHz. The $LCL$ filter parameters are $45\mu H$ for $L_{fs}$, $12\mu F$ for $C_f$ and $450\mu H$ for $L_{fg}$. C3M0021120K SiC from Cree and TMS320F28379D from TI are applied for switches and controller, respectively.
7.4.1 Third Harmonic Injection Test

The regulated third harmonic injection methods are validated in Fig. 7.7 and Fig. 7.8(a). Specifically, the sinusoidal RTHI in Fig. 7.7 achieves a voltage gain of 1.13 and the triangular RTHI in Fig. 7.8(a) achieves a voltage gain of 1.12, respectively. Also, the transient waveforms from Sin-RTHI and Tri-RTHI modes to constant zero-sequence voltage (Const-$v_0$) mode are shown in Fig. 7.9 and Fig. 7.10, respectively. The voltage gain, THD, third harmonic percentage of capacitor voltage, grid current/voltage and leakage current performance of the proposed Sin-THI, Tri-THI and Const-$v_0$ methods are compared with conventional THI (Con-THI) and no THI cases which are shown in table 7.1. The proposed RTHI methods can improve the DC bus utilization by 12% to 13%. The grid current/voltage THD are maintained within 1.5% with the proposed RTHI with less than 3% of third harmonics to be injected to the grid. However, the conventional THI method deteriorates the grid THD to be larger than 15% with more than 15% of third harmonics to be injected to the grid. Thus, compared with the Con-THI, the proposed RTHI methods can achieve maximum voltage gain with lowest grid current/voltage THD and minimum third harmonic components which means the RTHI can avoid the harmonics to be injected to the grid.
Figure 7.11: The leakage currents and common mode voltages in Sin-RTHI, Tri-RTHI, Constant-$v_0$, proposed topology without Constant-$v_0$ control and conventional modes.

7.4.2 Leakage Current Test

The common mode voltage and leakage current waveforms of the Sin-RTHI, Tri-RTHI, Const-$v_0$ and non-THI are shown in Fig. 7.11. Also, the leakage current values are summarized in table

<table>
<thead>
<tr>
<th>Topology</th>
<th>Sin-RTHI</th>
<th>Tri-RTHI</th>
<th>Const-$v_0$</th>
<th>Con-THI</th>
<th>No THI</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_v$</td>
<td><strong>1.13</strong></td>
<td><strong>1.12</strong></td>
<td>1</td>
<td>1.11</td>
<td>1</td>
</tr>
<tr>
<td>$THD_{vc}$</td>
<td>15.3%</td>
<td>17.6%</td>
<td>2.3%</td>
<td>18.5%</td>
<td>2.5%</td>
</tr>
<tr>
<td>$THD_{ig}$</td>
<td><strong>1.2%</strong></td>
<td><strong>1.4%</strong></td>
<td><strong>1.3%</strong></td>
<td>17.4%</td>
<td>1.6%</td>
</tr>
<tr>
<td>$THD_{vg}$</td>
<td>0.93%</td>
<td>1.1%</td>
<td><strong>0.91%</strong></td>
<td>15.3%</td>
<td>1.2%</td>
</tr>
<tr>
<td>$v_{c3rd}$ %</td>
<td>10.2%</td>
<td>13.5%</td>
<td>1.5%</td>
<td>17.6%</td>
<td>1.8%</td>
</tr>
<tr>
<td>$i_{g3rd}$ %</td>
<td>2.1%</td>
<td>2.9%</td>
<td>2.7%</td>
<td>16.3%</td>
<td>2.6%</td>
</tr>
<tr>
<td>$v_{g3rd}$ %</td>
<td>1.6%</td>
<td>1.7%</td>
<td>1.5%</td>
<td>16.7%</td>
<td>1.2%</td>
</tr>
<tr>
<td>$i_{lkg}$ mA</td>
<td>13.3mA</td>
<td>14.5mA</td>
<td>12.7mA</td>
<td>416mA</td>
<td>392mA</td>
</tr>
</tbody>
</table>

Table 7.1: The comparison of proposed and conventional methods.
7.1. The zero-sequence voltage is controlled by the MPC to be half of DC bus voltage in Const-
v_0 mode and with the injected third harmonic components in Sin-RTHI and Tri-THI modes. The
leakage current are all limited to be within 15mA for the three modes which are 30 times lower than
the conventional method. Thus, both the common mode voltage and current are compliant with the
UL and IEC standard requirements. Also, to further study the independent effects of zero sequence
voltage control and the modified topology on the reduction of leakage current, the leakage current
and common mode voltage of the modified topology without zero sequence voltage control have
been shown in Fig. 7.11 where the leakage current is 80mA. Thus, both the zero sequence voltage
control and modified topology contribute to the leakage current reduction. The modified topology
attenuates 5 times of the leakage current compared with the conventional topology. Furthermore,
the zero sequence voltage control reduces another 5 times of the leakage current compared to the
modified topology without zero sequence control case.

7.5  Summary

This chapter proposes a modular model predictive control method for a novel non-isolated
three-phase DC/AC converter with the capabilities of zero-sequence voltage stabilization and reg-
ulated third harmonic injection. The proposed non-isolated topology is designed to connect the
common point of three-phase LCL capacitors and positive/negative DC bus terminals to bypass
the zero-sequence leakage current. The zero-sequence voltage MPC controller stabilizes the zero-
sequence capacitor voltage to be a constant of half DC bus. Thus, the leakage current flowing
through the grid is attenuated. The proposed regulated third harmonic voltage injection methods
improve the DC bus utilization. By adding the third harmonic to the zero-sequence voltage MPC
reference, the stability and robustness are improved. And compared to the traditional THI meth-
ods in the aspect of grid THD, the grid power quality is improved since no extra harmonics are
injected to the grid and there is no need for optimization algorithm to reduce the grid THD. Per
phase explicit modular MPC simplifies the execution complexity on DSP and does not need to
update the angular speed in the state space matrix which makes it possible to implement the MPC
optimization offline. Compared with the traditional PI controller, the proposed MPC improves the
dynamic performance and control bandwidth with faster response. Compared with the traditional
MPC controller, no grid side inductance value is needed for the two-layer cascaded control struc-
ture which both improves the dynamic performance from inner MPC loop and avoids the MPC
parametric error caused by the uncertainty of grid side inductance.
Chapter 8: Conclusion and Publications

8.1 Conclusion

This dissertation presents the design and development of software-defined power electronics architecture to abstract the electrified energy conversion system by leveraging advanced control, estimation and magnetic optimization methods. For the application-oriented power electronics problems, the developed software-defined architecture generalizes the power electronics design procedures with a reconfigurable multi-layer concept. Various types of electrified load/source have been applied to the proposed system.

The variable-frequency critical-soft-switching control method is developed for the local power module to replace the high turn-on loss with low turn-off loss. Both DC/DC converter and DC/AC inverters are validated with the proposed method. The VF-CSS contributes to the efficiency improvement of 3%.

A high performance inductor design method is developed to enable mega-hertz frequency critical-soft-switching for high efficiency and power density. The most crucial magnetic component of switch side inductor is optimized with litz type of PCB winding and adjustable core structures. A neural network model is leveraged to analyze the performance of litz PCB winding loss. The designed inductors have been compared with the existing commercial inductors and showed the advantages of 4 times less loss, 40% less volume and 50°C less temperature rise.

A modular model predictive control method is designed to improve the dynamic performance and reduce the oscillation caused by the variable-frequency critical-soft-switching operation. The developed modular MPC increases the control bandwidth with higher reference tracking speed and less overshoot issue.

A hierarchical software-defined power electronics architecture is proposed based on the MPC
and VF-CSS for local power module and high level control functions to generalize the electrified energy conversion system and improve the power converter performance. Several merits are achieved including: (1) generalized design procedures to reduce the repetitive power electronics design processes; (2) reconfigurable architecture to form different power converter topologies with the corresponding control functions; (3) wide application interfaces to be applicable for various types of electrified load/source; (4) redundant mechanism with self-healing to diagnose and substitute the fault circuit components. Based on the generalized architecture, several design cases have been implemented experimentally including isolated/non-isolated DC/DC converter, grid-tied inverter, battery charger and motor traction inverter to validate the feasibility of the proposed concept.

A high efficiency and power density grid-tied inverter is designed based on the VF-CSS and modular MPC to achieve an efficiency above 99% at the rated power of 15kW and a power density of 10.4kW/L. The designed litz PCB winding inductor is leveraged to be combined with the VF-CSS to achieve more than 1MHz switching frequency. The modified power module combined with a zero-sequence voltage control method enables a non-isolated inverter topology with low leakage current and low cost.

An MPC-based regulated third harmonic injection technique is developed for the improvement of DC bus voltage utilization in a modified zero-sequence stabilized \( LCL \) inverter. The proposed MPC-based regulated third harmonic injection method is implemented through zero-sequence voltage reference tracking. The output voltage/current distortion is largely attenuated and the robustness is improved compared to the conventional third harmonic injection methods. Also the computation burden is decreased without the need of extra output distortion optimization algorithms.

8.2 Publications

Google Scholar link available at
https://scholar.google.com/citations?user=U2y3pVsAAAAJ&hl=en&oi=ao
8.2.1 Journals


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* * *


8.2.2 International Conferences


8.2.3 Patents

References


C. A. Aragon, R. Guzman, L. G. de Vicuña, J. Miret, and M. Castilla, “Constrained predictive control based on a large-signal model for a three-phase inverter connected to a


