Integrated and Distributed Digital Low-Drop-Out Regulators with Event-Driven Controls and Side-Channel Attack Resistance

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Abstract

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A modern system-on-chip (SoC) integrates a range of analog, digital, and mixed-signal building blocks, each with a dedicated voltage domain to maximize energy efficiency. On-chip low-drop-out regulators (LDOs) are widely used to implement these voltage domains due to their advantages of high power density and the ease of integration to a complementary metal-oxide-semiconductor (CMOS) process.

Recently, digital LDOs have gained large attention for their low input voltage support for emerging sub-mW SoCs, portability across designs, and process scalability. However, some of the major drawbacks of a conventional digital LDO design are (i) the trade-off between control loop latency and power dissipation which demands a large output capacitor, (ii) failure to address the performance degradations caused by the parasitics in a practical power grid, and (iii) insufficient power-supply-rejection-ratio (PSRR) and large ripple in the output voltage.

Chapters 2 through 4 of this thesis present my research on the design and circuit techniques for improving the aforementioned challenges in fully-integrated digital LDOs. The first work implements a hybrid event- and time-driven control in the digital LDO architecture to improve the response and settling time-related metrics over the existing designs. The second work presents a power delivery system consisting of 9 distributed event-driven digital LDOs for supporting a spatially large digital load. The proposed distributed LDO design achieves large improvements in the steady-state and non-steady-state performances compared to a single LDO.
design. In the third work, we prototype a digital LDO based on new current-source power-FETs to achieve a high PSRR and low output voltage ripple.

Lastly, on-chip voltage regulators have recently found usefulness in hardware security applications. An on-chip LDO can be used to improve the side-channel attack (SCA) resistance of a cryptographic core with design modifications to the classical LDO architecture. However, the existing designs incur non-negligible overheads in performance, power, and silicon area due to the conventional active-for-all-encryption-rounds architecture. In the last chapter, we propose a detection-driven activation technique to achieve a near-zero energy-delay-product (EDP) overhead in a SCA resilient digital LDO. In this architecture, the LDO can detect an attack attempt and enable SCA protection only if an attack is detected.
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Chapter 1: Introduction

Advances in complementary metal-oxide-semiconductor (CMOS) technology have allowed integrating increasingly more modules, e.g. a digital core, memory, I/O, and analog/RF block, in a system-on-chip (SoC). As shown in Figure 1.1, a low-drop-out regulator (LDO) is commonly used to create an independent voltage domain for each module. Such multi-domain power management is key to saving power as each voltage domain can be configured to its maximum energy efficiency point. Also, implementing integrated LDOs allows for fast per-core dynamic voltage scaling (DVS) to dynamically track the maximum energy efficiency over time.

1.1 Analog vs. digital LDOs

Energy-efficient operation is crucial in a wide range of modern electronic systems ranging from high-performance computing to Internet-of-Things (IoT) devices. One of the widely used techniques to improve energy efficiency is the operation of circuits in near-threshold voltage (NTV). A conventional analog LDO can achieve fast response time against output
voltage ($V_{OUT}$) variations and small output voltage ripple at nominal super-threshold voltage. However, its dynamic load regulation performance quickly degrades at NTV because it becomes increasingly challenging to design analog hardware with large gain and high bandwidth with limited voltage headroom.

In comparison, digital LDOs recently gained popularity due to their low input voltage ($V_{IN}$) supportability, portability, as well as process scalability. Figure 1.2 shows the conventional architectures of an analog LDO and a digital LDO [1]. A digital LDO replaces the analog error amplifier with a synchronous comparator and a digital controller, which generates an n-bit digital output. Also, instead of implementing a single PMOS power-FET that receives an analog gate voltage, the digital LDO uses a switchable n-bit PMOS power-FET array to provide current to the load ($R_{LOAD}$).

While the PMOS used in the analog LDO is typically biased in the saturation regime for high loop gain, the PMOS array in the digital LDO commonly operates in the linear regime. Therefore, digital LDOs can more easily support lower dropout voltages (the difference between the input voltage and the output voltage) than the analog counterparts.

Figure 1.2: Conventional (a) analog and (b) digital LDO.
1.2 Dynamic load regulation

![Diagram of Dynamic Load Regulation](image)

**Figure 1.3: Digital LDO’s dynamic load regulation performance.**

One of the most important performance metrics of an LDO is its load transient response, which is also known as the dynamic load regulation. The dynamic load regulation is a measurement of how much an LDO can keep the $V_{OUT}$ constant against a fast and large load current change.

For example, as shown in Figure 1.3, a sharp and large increase in the load current induces a voltage droop ($V_{DROOP}$) in the $V_{OUT}$ of the LDO from the target reference voltage ($V_{REF}$). The equation for $V_{DROOP}$ can be formulated as below:

$$V_{DROOP} \approx \frac{\Delta I_{LOAD} \cdot T_{lat}}{C_{OUT}}$$ \hspace{1cm} (1.1)

where $I_{LOAD}$ is the load current, $T_{lat}$ is the control loop latency, and $C_{OUT}$ is the output capacitor.

It is crucial to always keep $V_{OUT}$ above the critical voltage ($V_{critical}$) of the load. Therefore, for a fixed $C_{OUT}$ size, we need to shorten $T_{lat}$ to ensure that the $V_{OUT}$ always stays above $V_{critical}$. In a conventional digital LDO, we can shorten the $T_{lat}$ by implementing a higher operating clock frequency ($F_{CLK}$) for the comparator and the digital controller. However, this indeed imposes a trade-off with power consumption.
The two most commonly used Figure-of-Merits (FoM) to evaluate a LDO’s dynamic regulation performance are the ps-FoM [2] and the pF-FoM [3] as shown below, where $I_Q$ is the quiescent current of the LDO.

$$\text{FoM [ps]} = C_{OUT} \cdot \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \cdot \frac{I_Q}{I_{LOAD}}$$  \hspace{1cm} (1.2)

$$\text{FoM [pF]} = C_{OUT} \cdot \frac{\Delta V_{OUT}}{V_{OUT}} \cdot \frac{I_Q}{\Delta I_{LOAD}}$$  \hspace{1cm} (1.3)

The ps-FoM (equation 1.2) aims to capture the trade-off between the LDO’s pseudo response time and current efficiency. The pF-FoM (equation 1.3) computes the trade-off between output capacitor size, normalized voltage droop, and pseudo current efficiency. A smaller FoM is better for both equations. It is worthy to note that the $V_{DROOP}$ performance is also a strong function of the edge time of the load current change ($T_{EDGE}$), $V_{IN}$, and process node. However, the above two FoMs do not account for these parameters.

Another important dynamic load regulation metric is the setting time ($T_S$). $T_S$ is defined as the time it takes for an LDO to recover $V_{OUT}$ back to $V_{REF}$ upon a load current change (Figure 1.3). The equation for the worst-case $T_S$ can be formulated as shown below:

$$T_S \approx \frac{1}{F_{CLK}} \cdot 2^{N_{PWR}},$$  \hspace{1cm} (1.4)

where $N_{PWR}$ is the bit count of the digital controller output or the resolution of the power-FET array. To improve $T_S$, we can implement a faster $F_{CLK}$, but this comes at the cost of increased power consumption. We can also reduce $N_{PWR}$, but this hurts the LDO’s accuracy performance, which will be discussed further in the next section.
1.3 Steady-state performances

Figure 1.4 illustrates the digital LDO’s accuracy performances in the steady state condition. A conventional digital LDO exhibits an intrinsic voltage ripple \( (V_{\text{ripple}}) \) in the steady-state, also known as limit-cycling. This is mainly caused by the quantization error of the single-bit voltage comparator in the digital LDO architecture. The digital controller is forced to update the output at every clock cycle because a comparator will always latch a +1 or -1.

It is also possible that a digital LDO will exhibit steady-state error, which is defined as the difference between \( V_{\text{REF}} \) and the average output voltage over time (\( V_{\text{OUT,avg}} \)). We can improve the steady-state error by increasing the \( N_{\text{PWR}} \) for a target maximum \( I_{\text{LOAD}} \). In other words, we can reduce the size of the unit transistor current of the power-FET array to improve the LDO’s accuracy. However, this comes at the cost of reduced dynamic load regulation performance as described in equation 1.4.

1.4 Power-supply-rejection-ratio

One of the major drawbacks of a conventional digital LDO is its insufficient power-supply-rejection-ratio (PSRR). This is due to its operation of the power-FET array in the linear
regime, which causes any noise in the $V_{IN}$ to directly penetrate to the $V_{OUT}$. The equation for the PSRR is shown below:

$$PSRR \ [\text{dB}] = 20 \cdot \log \left( \frac{\Delta V_{OUT}}{\Delta V_{IN}} \right)$$ (1.5)

Figure 1.5 shows the first order illustration of the PSRR performance of a digital LDO. The low-frequency noise is typically handled by the active feedback loop of the digital LDO to stabilize the $V_{OUT}$. The high-frequency noise, on the other hand, is mainly compensated through the output decoupling capacitor.

### 1.5 Current and power efficiency

Achieving high current and power efficiencies is crucial in designing digital LDOs. Below shows the equation for the current efficiency:

$$\text{current efficiency} \ [\%] = \frac{I_{LOAD}}{I_Q + I_{LOAD}} \cdot 100$$ (1.6)

Here, the summation of $I_Q$ and $I_{LOAD}$ is the total current consumed by the LDO and the load. Recent digital LDO designs can achieve a maximum current efficiency of above 99.9%. In comparison, the minimum current efficiency is obtained at the minimum $I_{LOAD}$ condition. Therefore, the minimum $I_{LOAD}$ is bounded by a target minimum current efficiency for a given $I_Q$ of a digital LDO.
The equation for the LDO’s power efficiency is shown below:

\[
\text{power efficiency} = \left( \frac{I_{\text{LOAD}}}{I_Q + I_{\text{LOAD}}} \right) \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}}} \cdot 100 = \left( \frac{I_{\text{LOAD}}}{I_Q + I_{\text{LOAD}}} \right) \cdot \frac{V_{\text{IN}} - V_{\text{DROPOUT}}}{V_{\text{IN}}} \cdot 100 \tag{1.7}
\]

As expected, it is a linear function of the ratio between \( V_{\text{OUT}} \) and \( V_{\text{IN}} \). Therefore to achieve higher power efficiency, we can reduce the dropout voltage \( V_{\text{DROPOUT}} \). However, reducing \( V_{\text{DROPOUT}} \) lowers the \( V_{\text{DS}} \) across the LDO’s power-FET array and thereby reduces the current density of the LDO.

**1.6 Impact of parasitics**

In practical applications, non-negligible parasitics in the power grid of the load can negatively impact the LDO performances. Therefore, it is paramount to account for these parasitics especially for a digital load that has been quickly increasing in terms of both silicon area and current demand. In particular, the parasitic resistance \( R_G \) of the power grid can significantly degrade the LDO’s steady state and load transient performances (Figure 1.6).

In the steady-state, the \( R_G \) induces an IR drop between the output of the LDO and the local point of a load because the power-FET current has to flow through the \( R_G \). This IR drop degrades the performance of the load, and in the worst case can cause critical timing violations.
that can lead to circuit failure. This IR drop problem becomes proportionally worse with increasing power grid size and current draw of the load.

The $R_G$ also worsens the dynamic load regulation performance. This is because the LDO can detect the $V_{DROOP}$ only after the parasitic RC delay of the power grid once a local load (potentially located far away from the LDO) suddenly draws a large current. During this time, the $V_{DROOP}$ is further developed. Even after the LDO detects the $V_{DROOP}$, the $R_G$ exacerbates the problem as it impedes the LDO’s power-FET current flow through the power grid. Therefore, the LDO cannot immediately provide a large current to a load to compensate for the $V_{DROOP}$.

Current practice to mitigate these problems is to add a guard-band above the target $V_{REF}$, so that the minimum $V_{OUT}$ never falls below $V_{critical}$. However, doing so degrades the power efficiency of the regulator and the load.

1.7 Applications in hardware security

Recently, integrated LDOs have found applications in the hardware security space. Hardware encryption engines, e.g. an Advanced Encryption Standard (AES) core, leak side-channel information such as power and delay. This information can be exploited by an adversary to perform side-channel attacks (SCA) to disclose the internal secret key.

One of the common methods that an attacker can hack an encryption core is through the correlation power analysis (CPA) attack. To perform the CPA, the attacker simply inserts a shunt resistor between the power supply and the encryption core and captures the power traces through an oscilloscope. The attacker then collects up to tens of thousands of these power trace samples for different plaintext and ciphertext pairs. Using these samples, the attacker performs a statistical analysis based on a power model of the encryption core to reveal its embedded secret key.
Figure 1. 7: CPA attack on (a) unprotected AES core vs. (b) protected AES core.

As shown in Figure 1.7, to combat against such power attacks, recent works [4, 5] have proposed to utilize SCA resilient LDOs to mask or distort the power traces/signatures to protect the encryption core. These countermeasures have shown to greatly improve the number of measurements-to-disclose (MTD) the secret key. However, the additional protection measures and modifications to the existing LDO architecture impose non-negligible overheads in performance, power, and area.

1.8 Organization of the thesis

Sections 1.1 through 1.7 discussed the background, performance metrics, design challenges, and applications of a digital LDO. The remainder of this thesis will discuss new circuit techniques and LDO architectures to improve the key performance metrics and address the design challenges. Chapter 2 presents a digital LDO architecture based on a hybrid event-and time-driven control for improving the dynamic load regulation performances. Chapter 3 presents a power delivery system based on 9 distributed event-driven digital LDOs to tackle the performance degradations caused by non-negligible parasitics in the power grid. Chapter 4 demonstrates a digital LDO based on a new power-FET structure for improving PSRR and $V_{\text{ripple}}$. 
Chapter 5 presents a SCA resilient digital LDO based on detection-driven current equalization with near-zero energy-delay-product (EDP) overhead. And lastly, we end this thesis in the conclusion.
Chapter 2: Fully Integrated Digital LDO based on Hybrid Event- and Time-Driven Control

This chapter presents a fully-integrated digital LDO with a 100pF $C_{OUT}$ in 65 nm CMOS process, based on a hybrid event- and time-driven control. Conventional time-driven LDOs achieve insufficient response time due to its trade-off with power consumption and the size of $C_{OUT}$. In contrast, event-driven LDOs exhibited a faster response time, yet with a much slower settling time. By combining the two controls, we aim to achieve both fast response and fast settling times for sharp and abrupt changes in $I_{LOAD}$, which in turn will enable $C_{OUT}$ scaling under a $V_{DROOP}$ constraint. The architecture employs a load-event-based triggered asynchronous feedforward controller, which operates in tandem with a synchronous feedback controller. The proposed LDO also implements a hysteresis clock switching control to largely scale down the $I_G$. Our LDO prototype improves the response time up to 5.7× and settling time up to more than 300× over the prior works.

2.1 Motivation

As compared to the well-known digital LDO work [1] published 10 years ago, modern synchronous (time-driven) LDOs [6-14] have made significant improvements in the load transient performances and silicon footprint. For instance, a recent work [6] has made a 5.3× improvement in the supported load current change ($\Delta I_{LOAD}$) with a 250× reduction in the $C_{OUT}$ size. However, the time-driven LDOs can only achieve limited response time ($T_R$). $T_R$ is defined as the time it takes for an LDO to counteract a $V_{OUT}$ undershoot or overshoot, which is approximately the time it takes to sample the first voltage error of the $V_{OUT}$ ($=V_{REF}-V_{OUT}$) and
Figure 2.1: Pulse generation and settling time performances of a conventional (a) time-driven digital LDO vs. (b) event-driven digital LDO.

update the controller output. For a classical time-driven LDO, this $T_R$ is bounded by the $F_{CLK}$. A long $T_R$ directly worsens the $V_{DROOP}$ and thereby demands a larger $C_{OUT}$.

On the other hand, voltage regulators based on continuous-time (CT) digital control were previously proposed, where [15] introduced an inductive DC-DC converter with CT-digital signal processing (DSP) to improve the load transient response. Also, inspired by the concept and technique of event-driven data acquisition and DSP [16-20], digital LDOs based on asynchronous (event-driven) control [21, 22] were proposed to achieve very short $T_R$. However, event-driven LDOs exhibit insufficient performance in the other important transient metric – settling time ($T_S$). $T_S$ is defined as the time it takes to recover from a $V_{DROOP}$ or voltage overshoot ($V_{OVERSHOOT}$). In dynamic voltage and frequency scaling (DVFS) [23, 24], a short $T_S$ is crucial to quickly switch between different $V_{OUT}$ levels. A recent event-driven LDO [21] reports a slow $T_S$ of 11.2μs, which is 3 orders of magnitude longer than its $T_R$ of 2.36ns (both measured at $V_{IN}$=0.5V). The main cause of the long $T_S$ is because updating an event-driven controller depends
on new triggers that are generated only if a plant state ($V_{OUT}$) considerably changes. As the LDO regulates the $V_{OUT}$ closer to the set point voltage ($V_{SP}$), however, the change in $V_{OUT}$ becomes increasingly slow. This gradually reduces the number of generated triggers and unavoidably slows down the $T_S$ (Figure 2.1). Also, event-driven control systems are complex to analyze and can cause an undesirable phenomenon known as sticking [22], where the $V_{OUT}$ settles at an incorrect voltage level due to a lack of generated triggers.

To address the aforementioned challenges, we investigate implementing both event- and time-driven controls in a digital LDO. Specifically, in this chapter, we propose a new LDO based on (i) hybrid event- and time-driven architecture and (ii) a hysteresis control for adaptive clock switching in the time-driven control. By employing both the event- and time-driven control loops, we aim to achieve short $T_R$ and short $T_S$. Some of the prior works have proposed digital LDOs with dual control loop controls [23, 24]; however, the novelty of this work is the load-event-based triggering of the asynchronous loop and its tandem operation with the synchronous loop. The proposed LDO was prototyped in a 65 nm CMOS process. Measurements demonstrate the effectiveness of the proposed control schemes, achieving large improvements in $T_R$, $T_S$, and $C_{OUT}$ over the prior arts [25].

### 2.2 Overall architecture

The proposed hybrid event- and time-driven digital LDO architecture is shown in Figure 2.2 (a). The architecture consists of two control loops: (i) the asynchronous slope-detection based feedforward loop (blue, top), which operates in tandem with (ii) the synchronous Proportional-Integral (PI) feedback loop (black, bottom). These two control loops are arbitrated by the clock/trigger controller. Specifically, it controls the triggering of the asynchronous feedforward controller, the clock generation, and the clock-state switching of the synchronous controller.
Figure 2. 2: (a) Proposed digital LDO architecture with a hybrid event- (blue) and time (black)-driven control, and (b) reference voltage levels used for the asynchronous feedforward controller (blue) and the synchronous feedback controller (black).

during a load regulation. Both a PMOS header array and a NMOS footer array are used in the asynchronous loop for immediately counteracting a $V_{DROOP}$ and $V_{OVERSHOOT}$, respectively.

Figure 2.2 (b) shows the reference voltage levels of the CT and discrete-time (DT) comparators used for the feedforward and feedback computations. The CT comparators [26] (marked as overshoot & undershoot detectors) trigger the asynchronous feedforward loop by detecting any significant changes in $V_{OUT}$ based on $Asyn_LV[1:0]$. On the other hand,
Syn_LV[6:0] defines the voltage error levels (or the difference from \( V_{SP} \)) that are used in the synchronous PI computation. The innermost comparators, Syn_LV[4:3], are used for creating the \( V_{SP} \) zone (or zero error zone) with 10mV resolution. As the proposed LDO architecture employs two control loops, the communication between these two controls is very important and will be discussed further in section 2.3.

### 2.3 Asynchronous feedforward and synchronous feedback controller operation

![Figure 2.3: Operation of the slope detection-based asynchronous feedforward controller.](image)

The operation of the feedforward controller is illustrated in Figure 2.3. Whenever \( V_{OUT} \) considerably deviates from \( V_{SP} \) (i.e. due to a \( \Delta I_{LOAD} \) event), the two CT comparators (Asyn_LV[1:0]) instantly detect this change. Then, the CT comparator outputs generate an asynchronous trigger in the feedforward controller for \( V_{OUT} \) slope detection. In the case of \( V_{DROOP} \), the slope detection is performed through an embedded 2-bit DT analog-to-digital converter (ADC) with voltage levels, Slope_LV[2:0] (Figure 2.4), which are nominally placed
Figure 2.5: Architecture of the synchronous feedback PI controller.

between \( Asyn\_LV[0] \) and \( Syn\_LV[2] \). It computes the slope of \( V_{DROOP} \) for one sample after a fixed time delay of \( \Delta t \) through the asynchronous trigger (\( Trig \)). The thermometer-coded output from the slope detector ADC (\( Slope\_LV[2:0] \)) is encoded to binary from a lookup table (LUT) to estimate the required new power-FET setting based on the steepness of the \( V_{OUT} \) slope. Then, it is multiplied with a gain (\( K_{FFP} \)) by a shifter, which activates its own set of power-FET array (\( PASYN[14:0] \) for the \( V_{DROOP} \) from Figure 2.2 (a)). This quickly compensates \( \Delta V_{OUT} \) before it deviates too much from \( V_{SP} \). For the case of \( V_{Overshoot} \), the feedforward controller performs the similar operation, but instead using a 1-bit embedded DT ADC for slope detection. The short latency of the asynchronous feedforward control loop significantly improves \( T_R \) and thus reduces \( V_{DROOP} \) and \( V_{Overshoot} \).

While the feedforward loop compensates for immediate undershoot or overshoot of \( V_{OUT} \), the synchronous feedback PI controller regulates \( V_{OUT} \) to \( V_{SP} \). Figure 2.5 shows the architecture of the feedback PI controller. At every positive clock edge, the DT-comparators (in Figure 2.2 (b)) discretize the \( V_{OUT} \) based on the error levels (\( Syn\_LV[6:0] \)) and send the outputs to a thermometer-to-binary error encoder (generating \( Error[6:0] \)) for PI computation. The P-part
Figure 2.6: Timing diagram of the asynchronous and synchronous controls regulating an abrupt $\Delta I_{LOAD}$ event.

compensates for the current error while the I-part accumulates the error through an adder at every negative clock edge (marked as $I_{PREV}$ register). The P-part and I-part values are added together to generate the synchronous feedback controller output, $PSYN[14:0]$, which updates the binary-sized PMOS headers (Figure 2.2 (a)).

Figure 2.6 shows the exemplary control waveforms showing the operation and communication between the asynchronous feedfoward and synchronous feedback controllers. The operation of these two parallel control loops requires transferring the control states, (i.e. power-FET settings), from the feedforward to the feedback controller. This is due to two reasons: (i) the power-FETs used for the asynchronous feedforward loop need to be reset to be ready to compensate for the next large $\Delta I_{LOAD}$ event and (ii) the feedforward computation result needs to be saved. To do so, the feedforward controller generates the feedforward error (50 in $FF_{Error}$ in Figure 2.6) based on the current asynchronous power-FET array setting (PASYN/NASYN). Then, the FF_Error is added to the registers that store the integration result ($I_{PREV}$) in the
synchronous PI controller at the first negative edge of the clock (i.e. 50 FF_Error is added to $I_{PREV}$). This operation is marked as a State Transfer in Figure 2.6. During this transfer, the power-FETs, PSYN[14:0], are updated at the exact same time when PASYN/NASYN[14:0] turns off (resets). State Transfer largely speeds up the I-part error accumulation time and significantly shortens $T_s$.

After the State Transfer process, the asynchronous control loop no longer triggers from additional event detection from the CT-comparators (Asyn_LV[1:0]) until the synchronous controller finishes the regulation (i.e. reaches steady-state). Otherwise, the LDO could exhibit undesired oscillations due to the reoccurring feedforward loop. To block additional triggering, the clock/trigger controller (Figure 2.2 (a)) asserts Trig_block (see Figure 2.6, where the undershoot detection no longer generates additional Trig). This also eliminates the risk of short circuit current through the PMOS header (PASYN[14:0]) and the NMOS footer (NASYN[14:0]), since the feedforward control only responds to either an overshoot or an undershoot event at one time. The asynchronous feedforward loop becomes ready to respond to the next new $\Delta I_{LOAD}$ event when the clock/trigger controller releases the Trig_block after it detects a steady-state. The steady-state detection and its implementation in the proposed hysteresis clock switching scheme will be discussed in detail in the next section.

2.4 Hysteresis control for adaptive clock switching

To save power, we implement an adaptive clock switching scheme in the synchronous control. It operates on a slow clock in the steady-state for saving $I_Q$, but switches to a fast clock for speed in the non-steady state. A prior work [12] has implemented a clock switching scheme, but it used only voltage level thresholds to switch between two clock speeds (Figure 2.7 (a)). Such a scheme, however, can create oscillations if one aims to use low clock frequency for the
Figure 2. 7: FSM of (a) prior voltage threshold-based states and (b) proposed voltage and error-based states.

Figure 2. 8: Waveform illustrating oscillations in (a) only voltage-based adaptive clock switching and no oscillations in (b) hysteresis control adaptive clock switching.
slow clock to save $I_Q$. For example, as illustrated in Figure 2.8 (a), the frequency of the slow clock ($F_{SLOW}$) is too low to sample the $V_{OUT}$ that rapidly crosses the two switching voltage level thresholds (between the Overshoot and Undershoot levels). Therefore, the controller repeatedly switches between the two clock speeds, making the system unstable.

To address this problem, we propose a hysteresis control for adaptive clock switching. As shown in the Finite State Machine (FSM) in Figure 2.7 (b), this scheme not only uses voltage thresholds, but also error thresholds to switch between two clock states. Specifically, the FSM allows an immediate transition from the Slow Clock to the Fast Clock state, but slows down the reverse transition with a state hysteresis. Figure 2.8 (b) depicts its operation. As soon as the undershoot detector detects a $V_{OUT}$ change, the FSM enters the Fast Clock state. Then, the controller forces to remain in the Fast Clock state until a steady state is detected. Steady-state detection is done by counting the number of consecutive zero error occurrences ($V_{OUT}$ is inside $V_{SP}$ zone) at each clock cycle (i.e. the $Steady\_CNT$ increments by 1 when $Error=0$ at the rising edge of $CLK$). When the count reaches a pre-defined threshold (e.g. 5), the controller considers that $V_{OUT}$ is in steady-state. This effectively creates a hysteresis in the Fast Clock to Slow Clock transition. While in the Fast Clock state ($F_{FAST}$), the system is able to sample the $V_{OUT}$ that rapidly transitions between two voltage level thresholds until $V_{OUT}$ fully stabilizes. This allows for the adaptive clock switching control to no longer limit the lower bound of $F_{SLOW}$. In this work, we can set $F_{SLOW}=1/2000\cdot F_{FAST}$, whereas the prior work [12] had to use $F_{SLOW}=1/10\cdot F_{FAST}$. 
2.5 Measurement results and comparison

Figure 2. 9: (a) Chip micrograph and (b) area breakdown of the prototype.

Figure 2.9 shows the photo of the prototype chip in a 65 nm process and area breakdown. The proposed LDO uses a 100-pF metal-oxide-silicon capacitor (MOSCAP) $C_{OUT}$. The reference voltages to the CT/DT-comparators are fed from an off-chip DAC, but can also be implemented with an on-chip R-string DAC and digital calibration. The load was implemented on the chip using a binary-sized NMOS transistor array, which was controlled using on-chip test circuits. Among the circuit blocks, the comparators and power-FETs are custom-designed, whereas the digital control block is synthesized and placed-and-routed through the standard-cell design flow. The standard-cell design flow makes it easier to port the design to other CMOS processes.

Figure 2.10 shows the measured load transient performances. For a $\Delta I_{LOAD}=1.76$mA with $<0.1$ns edge time ($T_{EDGE}$) from 500$\mu$A to 2.26mA, the proposed LDO achieves $T_R=2.63$ns, $T_S=37$ns, and $V_{DROOP}=46$mV at $V_IN=0.5V$ and $V_{OUT}=0.45V$ ($V_{SP}$ zone=0.45~0.46V), using $F_{FAST}=43$MHz and $F_{SLOW}=22$kHz (Figure 2.10 (a)). The light-load can be as low as 15$\mu$A. The proposed asynchronous feedforward control plays a crucial role, without which the LDO exhibits poorer response (Figure 2.10 (b)).
Figure 2. 10: Dynamic load regulation measurements (a) with the asynchronous feedforward controller and (b) without the asynchronous feedforward controller.

Also, the proposed LDO can support a range of $V_{IN}$s from 0.5 to 1V and a range of $V_{DROPOUT}$s from 0.05 to 0.15V. At higher $V_{IN}$s, the LDO achieves faster $T_R$, but at the cost of increased $I_Q$. Simulations show that at $V_{IN}$=1V, $V_{OUT}$=0.95V, and $\Delta I_{LOAD}/T_{EDGE}$=20mA/0.1ns, the LDO exhibits $V_{DROOP}$=91mV and $I_Q$=458µA. Also, at $V_{IN}$=0.75V, $V_{OUT}$=0.7V, and $\Delta I_{LOAD}/T_{EDGE}$=6mA/0.1ns, the LDO exhibits $V_{DROOP}$=47mV and $I_Q$=160µA.

We also measure the load transient performances across $\Delta I_{LOAD}$s (Figures 2.11 (a) and (b)). The asynchronous feedforward control improves $V_{DROOP}$ up to 2.8× and $T_S$ up to 42.2×.
Figure 2.11: Measurements for (a) $V_{DROOP}$ performances across $\Delta I_{LOAD}$, (b) $T_S$ performances across $\Delta I_{LOAD}$, (c) $T_S$ and $I_Q$ trade-off for proposed vs. single clock design, and (d) current efficiencies across $I_{LOAD}$.

Figure 2.11 (c) shows that the proposed adaptive clock switching improves $T_S$ by 36.1\times and $I_Q$ by 7.8\% over the same LDO operating at a single 12 MHz clock. The proposed LDO also achieves a peak current efficiency of 98.4\% (Figure 2.11 (d)). Lastly, we compare our proposed LDO with the recent designs reporting 0.5V-$V_{IN}$ measurements in Table 2.1. Our LDO improves the $T_R$ by 5.7\times and $T_S$ by 2.7\times over the prior time-driven LDOs [6, 12], and more than 300\times better $T_S$ over the prior event-driven LDOs [21, 22] at a comparable $T_R$. 

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Table 2.1: Comparison against prior works reporting 0.5V-$V_{IN}$ measurements.

<table>
<thead>
<tr>
<th>Control</th>
<th>[6]</th>
<th>[12]</th>
<th>[21]</th>
<th>[22]</th>
<th>This work [25]</th>
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<tr>
<td>Time-Driven</td>
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<td>Event-Driven</td>
<td>Event-Driven</td>
<td>Hybrid</td>
<td></td>
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<tr>
<td>Active Area [mm²]</td>
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<td>0.114</td>
<td>0.03</td>
<td>0.029</td>
<td>0.012</td>
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<tr>
<td>Process</td>
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<td>130nm</td>
<td>65nm</td>
<td>65nm</td>
<td>65nm</td>
</tr>
<tr>
<td>$V_{IN}$ [V]</td>
<td>0.5-1</td>
<td>0.5-1.2</td>
<td>0.45-1</td>
<td>0.5-1</td>
<td>0.5-1</td>
</tr>
<tr>
<td>$V_{OUT}$ [V]</td>
<td>0.3-0.45</td>
<td>0.45-1.14</td>
<td>0.4-0.95</td>
<td>0.45-0.95</td>
<td>0.35-0.95</td>
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<tr>
<td>$C_{OUT}$ [nF]</td>
<td>0.4</td>
<td>1</td>
<td>0.1</td>
<td>0.4</td>
<td>0.1</td>
</tr>
<tr>
<td>$I_{LOAD, MAX}$ [mA]</td>
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<td>4.6</td>
<td>3.356</td>
<td>0.33</td>
<td>2.8</td>
</tr>
<tr>
<td>$I_{O}$ [μA]</td>
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<td>24-221</td>
<td>8.1-258</td>
<td>12.5-216</td>
<td>45.2</td>
</tr>
<tr>
<td>Peak Current Efficiency [%]</td>
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<td>98.3</td>
<td>99.2</td>
<td>96.3</td>
<td>98.4</td>
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<tr>
<td>Power Efficiency [%]</td>
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<td>89.2</td>
<td>86.7</td>
<td>88.6</td>
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<td>$\Delta V_{OUT} @ \Delta I_{LOAD}$</td>
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<td>90mV @ 1.4mA</td>
<td>34mV @ 1.44mA</td>
<td>40mV @ 0.4mA</td>
<td>46mV @ 1.76mA</td>
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<tr>
<td>$T_{EDGE}$ [ns]</td>
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<td>N.R.</td>
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<tr>
<td>$T_{S}$ [μs]</td>
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<td>64.3</td>
<td>2.36</td>
<td>40</td>
<td>2.63</td>
</tr>
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</table>

* $T_{R} = C_{OUT} \times (\Delta V_{OUT} / \Delta I_{LOAD})$
N.R. = Not Reported
2.6 Summary

This chapter demonstrated a fully-integrated, 100pF-$C_{OUT}$, hybrid event- and time-driven digital LDO. It implements a load event-based triggered feedforward control and a feedback PI control with state-based hysteresis clock switching to improve the $T_R$ and $T_S$ related metrics. Upon a load change event detection, the feedforward controller immediately compensates for the output voltage change at short latency. Then, the synchronous feedback PI controller regulates the output voltage to the set point voltage with fast sampling. In the steady-state, the voltage and error-based FSM control with hysteresis clock switching allows implementing 3 orders of magnitude slower operating clock frequency, which significantly reduces the quiescent power consumption.
Chapter 3: A 0.5-1V Input Event-Driven Multiple Digital LDO System for Supporting a Large Digital Load

In this chapter, we design an on-chip power delivery hardware that can support a spatially large digital load with a large current demand. We find that classical single LDO designs are inadequate to support such loads due to the substantial performance degradations caused by the power grid parasitics. To address this, we propose a power delivery system comprised of nine event-driven digital LDOs. In particular, we aim to improve (i) the accuracy performance (IR drop) in the steady state and (ii) the dynamic load regulation performances. Also, to further improve the feedback control latency, we implement a novel domino sampling and regulation technique in each LDO. We prototyped a chip consisting of 3×3 of the proposed digital LDO in a 65-nm CMOS process. Our design achieves up to 45.3× improvement in the dynamic load regulation FoM and up to 8.7× larger current density as compared to the state-of-the-art single and distributed LDOs.

3.1 Motivation

In modern SoC designs, it has become crucial to support a digital load that has been rapidly increasing in terms of both current draw and silicon area (Figure 3.1). Recently, integrated digital LDOs have gained increasing attention due to their high current density and compact design. Many of the existing works [27-33], however, aimed to support small loads in the order of 1 to 10 mA. To support a larger load (in the order of 500mA or higher), it is not sufficient to simply increase the size of the power-FETs in the existing single-LDO architectures. This is due to the non-negligible parasitics in the practical power grid of a load. In particular, we investigate the effects of power grid resistance ($R_G$), which leads to mainly two problems.
The first problem is the IR drop ($V_{IR}$) across the power grid in the steady-state. Figure 3.2 (a) illustrates an exemplary simplified power delivery model. As the LDO provides the current to a load distant from the LDO (marked as the far load), its power-FET current ($I_{PWR}$) has to flow through the $R_G$. This inevitably causes the IR drop. The LDO, however, cannot correct this IR drop because it cannot sense the voltage at the far load. This IR drop problem becomes proportionally worse with larger power grid size and larger current draw. The current practice to address the IR drop is to add a guard-band above the set-point voltage ($V_{SP}$) to ensure that the $V_{OUT}$ at the far load always stays above $V_{critical}$ even with the worst-case $V_{IR}$, but this worsens the power efficiency.
Figure 3.2: Single LDO exhibiting (a) IR drop and (b) $V_{DROOP}$ problems caused by $R_G$ vs. (c) multiple LDO system with improved IR drop or $V_{DROOP}$ problems.

The second problem is the worse load transient response. For instance, consider the case when a far load suddenly draws a large amount of current (marked as a load event) and thereby causes a $V_{DROOP}$ (Figure 3.2 (b)). Since the LDO is located far away from the location of this load event, it can only sense the $V_{DROOP}$ after a parasitic RC delay. During this time, $V_{DROOP}$ is further developed until the LDO senses and responds. To make it worse, the LDO cannot effectively compensate the $V_{DROOP}$ even after it makes the detection because the $R_G$ impedes the
$I_{PWR}$ flow in the power grid. Therefore, the LDO cannot supply enough current immediately to match the far load’s current draw.

To address these $V_{IR}$ and $V_{DROOP}$ problems, a promising approach is to split an LDO into multiple smaller instances (or duplicate a smaller LDO) and distribute them spatially across the power grid. For example, as illustrated in Figure 3.2 (c), the single LDO can be divided into two smaller LDOs. Now, the two LDOs directly sense their local $V_{OUTs}$ and can immediately supply the current. By doing so, we can mitigate the aforementioned problems caused by $R_G$.

However, distributing multiple LDOs requires careful consideration. Implementing multiple LDOs consumes more power than the original single LDO (Figure 3.3 (a)). This is simply because each distributed LDO requires its own ADC and digital controller. In the conventional time-driven (TD) LDO architectures, we could reduce this power overhead by lowering the operating clock frequency, yet this degrades the dynamic load regulation performances.

A prior work [34] tackled this problem by interleaving the clock to each TD LDO to reduce the power overhead. Interleaving, however, hurts the worst-case $V_{DROOP}$ performance since it cannot ensure that the LDO that receives the next rising edge of the clock will be the one nearest to a local load event. In other words, the fixed sequence of interleaved clocks cannot address the random occurrence of load change events. Therefore, this leaves the worst-case latency to $\sim N$ clock cycles for an $N$ LDO system as shown in Figure 3.3 (b). During this long latency, neighboring or far LDOs cannot effectively assist in counteracting the $V_{DROOP}$ since $R_G$ impedes the current flow. Besides, interleaving requires to design each LDOs differently based on their placement and needs to distribute a global clock, preventing the LDO architecture from being modular.
Figure 3.3: Dynamic load regulation performance comparisons between 9 distributed (a) time-driven controls, (b) time-driven interleaved control, and (c) event-driven controls.

Another work [35] instead proposed a power delivery system with distributed micro regulators based on high-speed analog control hardware for improving $V_{DROOP}$. However, the design achieves only a low peak current efficiency of 77.5%. Also, it required implementing a
master global controller to coordinate the distributed micro regulators. Similarly to [34], such a centralized control prevents the LDO architecture from being modular.

In comparison, an event-driven (ED) digital LDO [36] was proposed to improve feedback loop latency at low power consumption. As shown in Figure 3.3 (c), an ED LDO is naturally a good candidate for the distributed architecture since it is guaranteed that the nearest ED LDO will always and immediately respond first to its closest load event, and therefore compensate $V_{DROOP}$ instantly. Additionally, it does not require global coordination since each ED LDO can make an autonomous decision as long as we can guarantee that it does not hurt the global stability. In section 3.7, we show that we can ensure global stability by properly setting the gains of control laws. Therefore, the ED control allows the LDO architecture to be highly modular, requiring neither placement based customization, centralized control hardware, nor global clock distribution. Last but not least, the distributed ED control hardware consumes minimal power as it stops updating the output in the steady-state.

For the above reasons, in this chapter, we investigate the design of distributed ED LDOs to support a large load [37]. Toward this goal, we first propose a novel domino sampling and regulation technique to significantly shorten the feedback latency in an ED controller of each LDO. Then, based on a framework to analyze the stability of distributed LDO systems, we determine how to distribute and configure those ED LDOs. In section 3.8, we present the prototype of the 3×3 digital ED LDO system in a 65-nm CMOS process, confirming the efficacy of the proposed techniques through measurements.

### 3.2 Single event-driven digital LDO architecture

The top-level architecture of the proposed single ED LDO is shown in Figure 3.4. Later in section 3.6, we will split/duplicate the proposed single LDO and then distribute them to
support a large load. The proposed ED LDO comprises of (i) a 2.6-bit ED ADC with an on-chip DAC providing the five reference voltage levels, (ii) a proportional (P) controller and an integral (I) controller with a local clock generator, and (iii) binary-sized P-part (P\textsubscript{OUT}\textsubscript{4}~P\textsubscript{OUT}\textsubscript{0}) and I-part (I\textsubscript{OUT}) power-FET arrays.

The ED ADC uses two CT and three DT comparators to discretize \(V_{OUT}\) into a thermometer-coded output (LV[4:0]). This output is then read by the P- and I-controllers, which update the power-FET settings to regulate \(V_{OUT}\) to \(V_{SP}\). \(V_{SP}\) is set between \(V_{REF}[3]\) and \(V_{REF}[2]\). The top three 6-bit PMOS header arrays (P\textsubscript{OUT}\textsubscript{0}[5:0], P\textsubscript{OUT}\textsubscript{1}[5:0], P\textsubscript{OUT}\textsubscript{2}[5:0]) are used for immediately counteracting \(V_{DROOP}\), while the bottom two 6-bit NMOS footer arrays (P\textsubscript{OUT}\textsubscript{3}[5:0], P\textsubscript{OUT}\textsubscript{4}[5:0]) are used for counteracting \(V_{OVERSHOOT}\). A 9-bit PMOS array is used for the I-controller.
3.3 Domino sampling and regulation

In digital LDO designs, conventional sampling can only achieve limited response times. For instance, Figure 3.5 (a) illustrates a timing diagram of the $V_{OUT}$ transient upon a $\Delta I_{LOAD}$ event in the LDO based on a conventional digital control system. In conventional sampling, even for the best case when the system samples the $V_{OUT}$ immediately after the $\Delta I_{LOAD}$ event, the system still requires to sample multiple times to compensate $V_{DROOP}$. This is because, at the first clock pulse, the sampled value is small ($LV[2:0]=100$) and the LDO increases the power-FET current only marginally. At the second rising edge of the clock, the LDO now samples a larger value ($LV[2:0]=111$) and provides a larger power-FET current. This shows that even if the LDO makes the first sample with short latency, it still requires multiple cycles to compensate for a $V_{DROOP}$, resulting in a long response time. To improve this, one needs to implement both short-latency and high-frequency sampling in the feedback control system to reduce $V_{DROOP}$ (Figure 3.5 (b)). However, short-latency and high-frequency sampling increase power dissipation and hardware complexity.
To address these challenges, we propose a technique titled domino sampling and regulation. The proposed ED ADC performs the domino sampling. As shown in Figure 3.6 (a), two CT comparators (CMP[2], CMP[3]) are used for the dead-zone ($V_{LSB}=V_{REF[3]}-V_{REF[2]}$) and three auxiliary DT comparators (CMP[0], CMP[1], CMP[4]) are used for the outer voltage levels. As compared to conventional sampling where all the comparators sample at the same time, in the proposed ADC, each comparator sample in a sequence like a domino (Figure 3.6 (b)). For instance, if $V_{OUT}$ crosses the voltage level of CMP[2] (CMP[3]), it triggers the next comparator CMP[1] (CMP[4]) through an embedded ring oscillator. Then, the differential outputs of CMP[1] trigger the next comparator, CMP[0]. This allows the ADC to acquire more samples in the fast transient region, i.e. the domino sampling acquires 3 samples/period whereas conventional sampling acquires 1 sample/period, along with the short latency of the first ED sample.
Figure 3.7: Architecture of the (a) proposed domino P-controller vs. (b) prior P-controller.

It is worth noting that using both CT and DT comparators (Figure 3.6 (a)) can save power for the same ADC resolution in an ED LDO design. In the prior works [3, 21, 22, 36], the total $I_Q$ is dominated by the quiescent bias current ($I_{BAS}$) consumed by the CT comparators. Therefore in the proposed ADC, we employ only two CT comparators, CMP[2] and CMP[3], for the innermost voltage levels as the dead-zone and use DT comparators for the other voltage levels. Since the DT comparators only consume leakage in the quiescent state, our hybrid CT and DT design can reduce the ADC’s quiescent power dissipation by ~60% for the same resolution.

Also, we propose a new P-controller to process the domino samples more rapidly. In the prior conventional P-controller [3, 21, 22, 36] (Figure 3.7 (b)), the controller needs to first encode the ADC sample (LV[4:0]) from thermometer to binary (i.e. generating Error [3:0]), then buffer Error[3:0] at the $P_{pulse}$ edge generated by XOR-ing current and past ADC samples, and then perform a shifter multiplication with $K_P[1:0]$ to finally produce the output,

$$P_{OUT}[8:0] = K_P[1:0] \cdot Error[3:0]$$  \hspace{1cm} (3.1)

This generates the power-FET current of the P-controller ($I_{PWR,P}$), which is formulated below:

$$I_{PWR,P} = I_U \cdot P_{OUT}[8:0].$$  \hspace{1cm} (3.2)
where \( I_U \) is the unit current of the power-FET array.

Unlike the conventional P-controller architecture, the proposed domino architecture (Figure 3.7 (a)) bypasses the thermometer-to-binary encoding process and computes \( P_{OUT}[8:0] \) directly from the ADC output (LV[4:0]). This is done by dividing the P-controller into five slices, where each is activated directly by its corresponding comparator output. Each slice produces a 6-bit partial output based on a pre-computed error value (\( P_{ERROR0-4} \)). For instance, the partial output of the 0-th slice is formulated as \( P_{OUT0}[5:0] = K_P[1:0] \cdot P_{ERROR0}[2:0] \), where \( P_{ERROR0} \) is configured based on \((V_{REF1}-V_{REF0})/V_{OUT} \cdot I_{LOAD}/I_U \). This partial output directly controls its corresponding (0-th) power-FET array (\( P_{OUT0}[5:0] \)). In the proposed architecture, the critical path is from LV[4:0] to \( P_{OUT}[5:0] \), reducing the latency down to only a single C-Q delay of a flip-flop. This is because the shifter based \( K_P \) multiplication is off the critical path and the inputs to the flip-flops are ready before the rising edge of LV[4:0]. Finally, the currents of these 5 power-FET arrays (\( P_{OUT0-4} \)) are combined. The total current of the P-controller power-FET arrays in the proposed architecture is formulated below:

\[
I_{PWR,P} = \sum_{n=0}^{4} K_P \cdot P_{ERRORn} \cdot I_U
\] (3.3)

### 3.4 CT and DT comparator circuits

The ED ADC implements custom-designed CT and DT comparators and an on-chip embedded DAC. The CT comparator design is based on [17] to implement on-chip self-calibration. The schematic of the proposed CT comparator is shown in Figure 3.8. The comparator sequentially takes in two inputs (\( V_{OUT} \) and \( V_{REF} \)) and produces a 1-bit output (LV). One of the key drawbacks of a conventional CT comparator is that it cannot support a wide range of supply voltage (\( V_{IN} \)), e.g., from 0.5V to 1V, while maintaining low power consumption. In
other words, the comparator either consumes a large crowbar current or becomes slow at the $V_{IN}$ that it is not designed for [3, 21, 22, 36]. To address this, we design a comparator whose bias current (strength) can be digitally-configured post-silicon. The comparator comprises of 5 binary-sized parallel inverter chains controlled through power gating switches. Its latency and $I_Q$ performance across different strength settings at $V_{IN}=0.5V$ and 1V is shown in Figure 3.9. With this configurability, the CT comparator can achieve optimal latency and $I_Q$ performances across $V_{IN}=0.5$ to 1V.
The CT comparator also performs self-calibration on-chip [17, 38]. To do so, it operates in two phases – the calibration phase and the comparison phase. In the calibration phase (rstb=0), the input capacitor (C_{IN}) is shorted to V_{REF}. Also, the input and output of the three cascaded inverter voltage amplifier are shorted, which biases the amplifier’s input voltage to the tripping voltage ($V_{TRIP} = \sim 0.5 \cdot VDD$) for maximizing the voltage gain. The voltage offset ($V_{OS}$) between \(V_{REF}\) and \(V_{TRIP}\) is then stored in C_{IN}. However, due to the charge leak of the C_{IN}, the comparator requires brief periodic recalibration. To reduce the required recalibration frequency, we implement C_{IN} with a 4-pF metal-insulator-metal (MIM) capacitor, with which we can use a low frequency of 25kHz. During the calibration phase, the digital controllers ignore the CT comparators’ LV value to avoid processing incorrect results. Next, in the comparison phase (rstb=1), C_{IN} is shorted to V_{OUT} and the input and output of the inverter amplifier are disconnected. The voltage difference, $V_{OUT} - V_{REF}$, is then amplified through the inverter chain, producing a rail-to-rail output (LV).

On the other hand, Figure 3.10 shows the schematic of the DT comparator. The first stage (M1~M5) has two inputs ($V_{OUT}$ and $V_{REF}$) and performs the comparison and pre-amplification of the differential input, generating $V_{XN}$ and $V_{XP}$. The difference between $V_{XN}$ and $V_{XP}$ is then amplified by the regenerative feedback in the second stage (M6~M13) to produce the rail-to-rail differential output signals (LV and LVB).

The DT comparator also performs on-chip calibration through a pair of 5-bit binary-sized capacitor banks at $V_{XN}$ and $V_{XP}$. The digital codes, C[4:0] and C’[4:0], control the discharging speed of $V_{XN}$ and $V_{XP}$ to calibrate the tripping point. The LSB of the capacitor bank is sized to give $\sim 3$ mV resolution control for the input-referred voltage offset.
3.5 Integral controller and steady-state detector

While the proposed P-controller achieves very short latency and good $V_{DROOP}$ and $V_{OVERSHOOT}$ performances, for guaranteeing zero (i.e., sub 1 LSB) steady-state error, the LDO must also accompany an I-controller. Therefore, in the design of the I-controller, we aim to improve $T_S$ and $V_{ripple}$.

In fact, the prior I-controllers based on ED control have exhibited unsatisfactory settling time performances [21, 22]. The root cause is due to the sticking problem, which is a phenomenon where the $V_{OUT}$ of an ED LDO updates gradually slowly as it approaches $V_{SP}$. In the case of a conventional TD LDO, we could improve $T_S$ by increasing the operating clock frequency. However, this not only increases power dissipation, but also makes $V_{ripple}$ large [12, 39].
Figure 3.11: Architecture of the I-controller based on event-driven clock-generator control.

Figure 3.12: Finite state machine for event-driven clock-generator control.

We aim to address this problem associated with $T_S$ and $V_{ripple}$ by combining several techniques in the I-controller design. First, we adopt the TD control but we also augment it with an ED local-clock-generator control. Specifically, we embed a local clock generator in the digital LDO to produce the clock for the I-controller ($I_{CLK}$) as shown in Figure 3.11. This local clock generator is enabled asynchronously by the CT comparators in the ED ADC and disabled synchronously by a steady-state detector in the clock-generator control finite state machine (FSM) shown in Figure 3.12. In this approach, since $I_{CLK}$ is enabled only when the $V_{OUT}$ is in non-steady-state, it saves clock power during the steady-state. Also, in the steady-state, the
controller’s output is not updated, which completely eliminates $V_{\text{ripple}}$ and confines the $V_{\text{OUT}}$ within the dead-zone.

The detailed operation of the FSM and the triggering of the proposed I-controller are as follows. From the Idle state, the FSM switches to the Active state as soon as $V_{\text{OUT}}$ crosses outside the dead-zone ($DZB=1$). This condition is detected asynchronously by the CT comparators, CMP[2] and CMP[3] (Figure 3.6 (a)). In the Active state, $I_{\text{CLK}}$ is enabled in the I-controller to perform the integral control. During this time, the I-controller samples $L V[4:0]$ at each $I_{\text{CLK}}$ cycle, and performs the thermometer-to-binary conversion, which is then multiplied with a gain ($K_I[1:0]$) using a shifter. The result is accumulated to the output, $I_{\text{OUT}}[8:0]$.

The FSM returns back to the Idle-state only if the steady-state detector finds the LDO is in the steady-state condition. To detect such condition, the steady-state detector checks if $V_{\text{OUT}}$ is within the dead zone ($DZB=0$) for $N$ consecutive $I_{\text{CLK}}$ cycles. In our design, $N$ can be programmable up to 16 cycles. Once the steady-state condition is met, $\text{STEADYB}$ becomes 0, which puts the FSM to the Idle state, disabling the local clock generator, and thereby stopping the I-controller from updating its output. Note that whenever $V_{\text{OUT}}$ crosses back outside the dead-zone while in the Active state, the FSM will restart the counting for checking the steady-state condition. This guarantees that the clock pulses are continuously generated without interruption until $V_{\text{OUT}}$ fully stabilizes to $V_{\text{SP}}$.

3.6 Overall architecture of distributed event-driven LDO system

In this section, we now duplicate the proposed ED LDO in section 3.2 and distribute them spatially to support the large target load. In this work, we assume that the entire load draws about 90mA from a 0.45V power supply (400mA from 0.9V) and that the power density of the
target load is spatially uniform. Since each ED LDO can support about 10mA at 0.5V $V_{IN}$ (about 46mA at 1V $V_{IN}$), we distribute nine of the LDOs uniformly. Also, since the proposed ED LDO is highly modular, multiple of them can work together to support a single load without centralized/explicit coordination and without having to redesign the LDO circuitries.

Figure 3.13 depicts the floor plan of the prototype chip where the nine identical LDOs are distributed in a 3×3 grid. Each LDO integrates a 0.1-nF $C_{OUT}$ (a total of 0.9-nF for the 9-LDO system). To emulate a range of a realistic power grid, we added a variable resistor ($R_G$) between every two LDOs whose resistance can be configured from 0.2Ω to 20Ω post-silicon.

### 3.7 Framework for global stability analysis

In the distributed LDO architecture, the power-FET current from each LDO can couple with the others’ through the power grid while each LDO does not know the actions of the other
Figure 3.14: Power delivery model of two LDOs regulating two local loads in a common power grid.

LDOs. In other words, each LDO does not know how much the other LDOs change their power-FET currents. This is a challenge because too large coupling can degrade the stability of the distributed system. Therefore, it is crucial to analyze the global stability of such a multi-LDO system and accordingly set the strength (i.e. gain parameters, $K_P$ and $K_I$) of the controllers of each LDO. To do so, we develop a state space representation of the multiple LDO system based on the $V_{OUT}$ dynamics and the controller settings between two consecutive samples/operations.

The multi-LDO forms a multi-input multi-output (MIMO) system [40, 41]. To simplify the analysis, we start with a system having two LDOs regulating two spatially distributed local loads ($R_{LOAD0}$, $R_{LOAD1}$) as shown in Figure 3.14. Here, each LDO regulates a local power grid voltage ($V_{OUT0}$, $V_{OUT1}$) and the two LDOs are distributed across a power grid with parasitic resistance, $R_G$. From one of the power nodes ($V_{OUT0}$), we can see that the system has four current paths – the power-FET current of the LDO[0] ($I_{PWR0}$), the load current ($V_{OUT0}/R_{LOAD0}$), the coupling current through the power grid ($I_R$), and the current that (dis)charges the $C_{OUT}$ of the LDO[0].

We formulate multiple state equations in this system. First, we can formulate $V_{OUT0}$ in the $(k+1)$-th time step as:
\[ V_{OUT0}(k + 1) = V_{OUT0}(k) + \left( I_{PWR0}(k) - I_R(k) - \frac{V_{OUT0}(k)}{R_{LOAD0}} \right) \cdot R_{LOAD0} \parallel R_G \cdot \left( 1 - e^{-T_P/(R_{LOAD0} \parallel R_G \cdot C_{OUT})} \right), \]  
(3.4)

where \( T_P \) is the time interval between two samples. We then formulate the voltage error of LDO[0] as:

\[ e_0(k) = \frac{V_{SP} - V_{OUT0}(k)}{V_{RES}}, \]  
(3.5)

where \( V_{RES} \) is the ADC resolution (the voltage difference between two adjacent reference levels).

Also, we can formulate the coupling current through the power grid (\( I_R \)) as:

\[ I_R = \frac{V_{OUT0}(k) - V_{OUT1}(k)}{R_G} \]  
(3.6)

And, we can formulate \( I_{PWR0} \) as:

\[ I_{PWR0} = G_0(k) \cdot I_U, \]  
(3.7)

where \( G_0(k) \) is the output of LDO[0]’s controller and \( I_U \) is the unit current of the power-FET array. Here, we can further formulate \( G_0(k) \) into:

\[ G_0(k) = K_P \cdot e_0(k) + I_0(k), \]  
(3.8)

where \( K_P \) is P-controller’s gain and \( I_0(k) \) is the I-controller’s output state. By combining the equations (3.4) to (3.8), we formulate the next error state \( e_0(k+1) \) as:

\[ e_0(k + 1) = \left( 1 - \left( \frac{K_P \cdot I_{LSB}}{V_{RES}} + \frac{1}{R_{LOAD0}} + \frac{1}{R_G} \right) \cdot A_0 \right) e_0(k) + \left( \frac{1}{R_G} \cdot A_0 \right) e_1(k) \]

\[ - \left( \frac{I_{LSB}}{V_{RES}} \cdot A_0 \right) I_0(k) + \left( \frac{1}{V_{RES} \cdot R_{LOAD0}} \cdot A_0 \right) V_{SP}, \]

where \( A_0 = R_{LOAD0} \parallel R_G \cdot \left( 1 - e^{-T_P/(R_{LOAD0} \parallel R_G \cdot C_{OUT})} \right) \)  
(3.9)

In (3.9), the integration state, \( I_0(k) \), is the accumulation of the error multiplied by the integral gain, \( K_I \). Therefore, we can formulate the next integration state \( I_0(k+1) \) as:

\[ I_0(k + 1) = I_0(k) + K_I \cdot e_0(k) \]  
(3.10)
\[
\begin{align*}
\begin{bmatrix}
e_0(k+1) \\
e_1(k+1) \\
A_1 \\
e_2(k+1) \\
L_2(k+1) \\
\vdots \\
e_B(k+1) \\
I_B(k+1)
\end{bmatrix} &= \begin{bmatrix}
1 - \left(\frac{K_P}{V_{RES}} + \frac{1}{r_{LOAD0}} + \frac{1}{r_G} \right) \cdot A_0 \\
\frac{A_0}{r_G} \cdot A_0 \\
\frac{A_1}{r_G} \cdot A_0 \\
\frac{A_1}{r_G} \cdot A_1 \\
\frac{A_2}{r_G} \cdot A_1 \\
\vdots \\
\frac{A_B}{r_G} \cdot A_B \\
\frac{A_B}{r_G} \cdot A_B
\end{bmatrix} - \frac{i_{LSB}}{V_{RES}} \cdot A_0 \\
\begin{bmatrix}
e_0(k) \\
e_1(k) \\
A_1 \\
e_2(k) \\
L_2(k) \\
\vdots \\
e_B(k) \\
I_B(k)
\end{bmatrix} + \begin{bmatrix}
A_0 \\
A_1 \\
A_2 \\
A_3 \\
A_4 \\
\vdots \\
A_B
\end{bmatrix} V_{SP} (3.11)
\end{align*}
\]
The equations (3.9) and (3.10) show the state space representation for the LDO[0]. We can also formulate the similar equations for LDO[1]. Then, we can rewrite the four equations into the matrix form as shown in equation (3.11). This represents the stability analysis framework for the 2-LDO system shown in Figure 3.14. Indeed, we can further expand the state space representation for the 3×3 LDO system as shown in equation (3.12). In this equation, $N_x$ is defined as the number of significant coupling paths from LDO[$x$] to any other neighboring LDOs.

As shown in Figure 3.15, we can then analyze the 9-LDO system stability by computing the eigenvalues of the state space matrix. The system is stable if all eigenvalues are inside the unit circle. We have explored the global stability for the following design parameters: $V_{IN}=0.5V,$
\[ V_{OUT} = 0.45V, \quad V_{RES} = 10mV, \quad I_U = 20\mu A, \quad C_{OUT} = 0.1nF, \] and a range of controller gains \((K_P, K_I)\). As expected, the system becomes more stable with smaller gain values (Figures 3.15 (a) and (b)). Also, the system becomes more stable with larger \(T_P\) values (Figure 3.15 (c)). In our analysis, we find that the system is stable for \(T_P = 1\sim4ns\). In our prototype, the minimum \(T_P\) is bounded by the control loop’s critical path delay and is set to >4ns for the P- and I-controllers at \(V_{IN} = 0.5V\). We also investigate various \(R_G\) values to evaluate its impact (Figure 3.15 (d)). We find that a larger \(R_G\) improves stability because it effectively decouples the impact of an LDO’s power-FET current on other LDOs. Based on this framework, we configure the \(K_P, K_I,\) and \(T_P\) on-chip to ensure stability, which is confirmed to be set appropriately by the test chip measurements in the next section (Figure 3.18).

### 3.8 Chip prototype and multi-LDO measurements

![Die photo of the proposed 3×3 ED LDO.](image)

Figure 3.16: Die photo of the proposed 3×3 ED LDO.

Figure 3.16 shows the chip micrograph of the proposed 3×3 ED LDO in a 65nm CMOS process. Each LDO integrates a \(0.156 \times 0.184\text{mm}^2\) MOS capacitor for \(C_{OUT}\) and the total active area of the 9 LDOs is \(0.067\text{mm}^2\). The 9-LDOs can support up to a total of 92.7mA (416.7mA) \(I_{LOAD}\) with a 10% drop-out voltage from the \(V_{IN}\) of 0.5V (1V), achieving a total current density of 248.8mA/mm\(^2\) (1.1186A/mm\(^2\)).
Figure 3.17: $V_{DROOP}$ and $V_{IR}$ performances for (a) single LDO vs. (b) multiple LDO system.

Figure 3.18: (a) Measured stability across controller gains ($K_p$, $K_i$, and $R_G$) and (b) measured $V_{IR}$ across 0.5V to 1V $V_{INS}$ for the proposed 3×3 LDO system.

Figure 3.17 shows the measured dynamic load regulation performance of the (a) single LDO vs. (b) multi-LDO. We emulate the single LDO case by only enabling LDO[4] and
disabling the others. For a sharp $\Delta I_{LOAD}$ of 9.2mA/0.2ns and $R_G=10\Omega$, the single LDO exhibits large a $V_{DROOP}$ of 163mV and a large $V_{IR}$ of 100mV. We see that the large $R_G$ negatively impacts the LDO response time and accuracy. On the other hand, the multi-LDO achieves 48.6mV $V_{DROOP}$ (3.4$\times$ reduction) and no $V_{IR}$ for the same $\Delta I_{LOAD}$, as the local LDO can immediately sense and regulate a local $\Delta I_{LOAD}$ event.

We test the stability of our multi-LDO system in Figure 3.18 (a). Measurement shows that at $V_{IN}=0.5V$ and $V_{OUT}=0.45V$, the system becomes more stable with decreasing $K_P$, $K_I$ and increasing $R_G$, which agrees with our analysis in section 3.7. We also measure the $V_{IR}$ performances across $V_{IN}=0.5$ to 1V (Figure 3.18 (b)). Our proposed system regulates all 9 $V_{OUTs}$ within a 2% steady-state error of $V_{IN}$ with $R_G=20\Omega$.

### 3.9 Single LDO measurements

Figure 3.19 shows the dynamic load regulation measurements for a single LDO regulating a local load. For a $\Delta I_{LOAD}$ of 4.04mA/0.1ns (13.8mA/0.2ns), the LDO exhibits a $V_{DROOP} = 49.8mV$ (94.1mV) = $\sim$11% of $V_{OUT}$ and $T_S = 122ns$ (135ns) at $V_{IN}=0.5V$ (1V).

From the measurements, we compute the ps-FoM [2] to examine the trade-off between passive size ($C_{OUT}$), $V_{DROOP}$, and $I_Q$. However, both dynamic load regulation and the FoM are strongly affected by the edge time ($T_{EDGE}$) of the $\Delta I_{LOAD}$, $V_{IN}$, and the technology node. Therefore, we measure the $V_{DROOP}$ and compute the FoM performances across $T_{EDGE}$s from 0.1ns to 30ns for $V_{IN} = 0.5V$ and 1V (Figure 3.20). We find that the $V_{DROOP}$ improves with increasing $T_{EDGE}$, and the FoM quickly improves at longer $T_{EDGE}$s and higher $V_{IN}$s, regardless of the circuit latency.
Figure 3. 19: Load transient responses of proposed single ED LDO at $V_{IN}=0.5$ and 1V.

Figure 3. 20: $V_{DROOP}$ and FoM performances of proposed single ED LDO across $T_{EDGE}$. 
Figure 3.21: Current efficiency of proposed single ED LDO across $I_{LOAD}$ and $V_{IN}$. The proposed LDO achieves a maximum current efficiency of 99.9% (99.8%) at $V_{IN}=0.5V$ (1V). The LDO maintains larger than 90% current efficiency for a 79× range in $I_{LOAD}$ at 0.5V $V_{IN}$. Thanks to the configurable CT-comparator design, the LDO achieves good current efficiencies across a wide $V_{IN}$ range.

Figure 3.22: DC load regulation performances of proposed single ED LDO across $V_{IN}$.
We also measure the DC load regulation performances in Figure 3.22. A single LDO can support up to 10.3 mA (46.3 mA) maximum $I_{LOAD}$ at 0.5V (1V) $V_{IN}$ with a 10% dropout voltage. The LDO regulates the $V_{OUT}$ to above $V_{SP}$ and within 1 LSB ADC resolution in the steady-state for all supported load current ranges. The LDO achieves good DC load regulation of 0.08~0.41mV/mA for $V_{IN}$=0.5~1V.

3.10 Comparison against prior art

Lastly, we compare our work to the prior single and multi-LDO works in Table 3.1. As compared to the multi-LDO work in 65nm [34], our design achieves 8.7× (2.8×) higher current density even with 0.1V (0.2V) lower $V_{IN}$. For dynamic load regulation, [34] only reports the FoM at a long $T_{EDGE}$ of 20ns. Among the designs reporting sub-ns $T_{EDGE}$, our proposed LDO achieves 3.9× and 45.3× FoM improvements over the prior ED [36] and TD [6] single LDO works, respectively. [42] achieves a comparable FoM of 4.45ps at 1.05V $V_{IN}$, but it is based on the TD-control and exhibits the power-latency trade-off of large $I_Q = 57,000\mu A$. 
Table 3.1: Comparison against prior single and distributed LDO designs.

<table>
<thead>
<tr>
<th>References</th>
<th>Single LDO</th>
<th>Distributed LDOs</th>
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<tr>
<td>Technology</td>
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<td>65nm</td>
<td>65nm</td>
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<tr>
<td>Control (# of LDOs)</td>
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<td>Time-driven (1)</td>
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<td>0.0001-1^*</td>
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<td>Peak current efficiency [%)</td>
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<td>Current density [mA/mm^2]</td>
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<td>ΔV_{OUT} [mV]</td>
<td>49.8</td>
<td>40</td>
<td>-</td>
</tr>
<tr>
<td>ΔI_{LOAD} [mA]</td>
<td>2.3</td>
<td>1.06</td>
<td>-</td>
</tr>
<tr>
<td>FOM [ps]</td>
<td>17.0</td>
<td>199.4</td>
<td>-</td>
</tr>
</tbody>
</table>

*Estimated from figures.

FOM = C_{OUT} (ΔV_{OUT}/ΔI_{LOAD})/(I_{Q} ΔI_{LOAD}), smaller FOM is better.
3.11 Summary

This chapter presented a 3×3 LDO system based on distributed ED controls and a novel domino sampling and regulation technique for regulating a spatially large digital load. By distributing ED LDOs, the nearest LDO can always and immediately respond to its local $\Delta I_{LOAD}$ event and thereby improve $V_{DROOP}$ and $V_{IR}$ significantly. The prototype in a 65nm process showed that the proposed design achieves 49.8mV (94.1mV) $V_{DROOP}$ for a $\Delta I_{LOAD}$ of 36.4mA/0.1ns (124.2mA/0.2ns) for $V_{IN} = 0.5V$ (1V) only with a $C_{OUT}$ of 0.1nF per each LDO. The proposed system can also be expanded to a larger n×m matrix without redesigning the LDO.
Chapter 4: A High PSRR, Low Ripple, Temperature-compensated, 10-µA-Class Digital LDO based on Current-Source Power-FETs for a Sub-mW SoC

In this chapter, we aim to address the insufficient PSRR and large $V_{\text{ripple}}$ problems in a classical digital LDO. To improve PSRR, we propose to use NMOS power-FETs biased in current-source configuration in place of the PMOS linear power-FETs. Then, to reduce the $V_{\text{ripple}}$, we employ a small power-FET unit current ($I_U$) and large power-FET resolution ($N_{PWR}$). Using large $N_{PWR}$, however, can slow down a controller’s regulation speed. Therefore, we infuse an event-driven initialization control in the digital controller for fast regulation. Based on these techniques, we prototyped a chip in 65nm CMOS, targeted for a sub-mW SoC. Measurements show that the design achieves -32dB PSRR at 1MHz, 2.6 (10.9) mV $V_{\text{ripple}}$ in the nominal (worst-case) condition, and a small $I_Q$ of 125.8nA with only a 50pF on-chip $C_{OUT}$.

4.1 Motivation

Modern IoT devices implement sub-mW SoCs for maximizing energy efficiency. A sub-mW SoC comprises of a range of digital and analog-mixed-signal (AMS) building blocks that consume only a few to hundreds of µW power at sub-1V supply [43, 44]. For regulating such loads, we need to design new power management circuit that will only consume a fraction of such load (10-100’s of nW), but still can provide an independent voltage on a chip with high accuracy and robustness. While a digital LDO is known for $V_{IN}$ and process scalability, many of the existing designs exhibit insufficient PSRR and large $V_{\text{ripple}}$.

As shown in Figure 4.1 (a), the main reason for low PSRR in conventional digital LDOs is due to the usage of PMOS digital power-FETs biased in the linear region, where its current...
**Figure 4.1:** Structure of (a) conventional linear PMOS digital power-FET vs. (b) proposed NMOS current source and digital PMOS switch.

\( I_{\text{PWR}} \) becomes quadratically-proportional to \( V_{\text{IN}} \). This leads to a large variability in \( I_{\text{PWR}} \). For instance, it exhibits 1.5\%/mV \( I_{\text{PWR}} \) variation in our simulation at \( V_{\text{IN}}=0.55\)V and \( V_{\text{DROPOUT}}=100\)mV (Figure 4.2 (a)). A prior work [45] tackled this PSRR problem by implementing high-bandwidth analog LDO tiles in parallel with digital LDO tiles. However, the analog LDO tiles have to compromise the \( V_{\text{IN}} \) scalability benefit (\( V_{\text{IN}}>1\)V) and increase the \( I_Q \)
consumption ($I_Q=27.4\mu A$). Likewise, another work [46] proposed to hybridize analog and digital controls for improving PSRR, but it suffers from similar problems.

Existing digital LDOs also exhibit large $V_{\text{ripple}}$ that is inadequate for noise-sensitive loads. The $V_{\text{ripple}}$ equation for a linear-biased PMOS power-FET is shown in Figure 4.1 (a). It is proportional to the $I_U$ times the $R_{\text{LOAD}}$. Therefore, since $I_U$ becomes largest at the maximum temperature and $R_{\text{LOAD}}$ becomes largest at the minimum load current condition (i.e., $I_{\text{LOAD}}=I_{\text{LOAD, min}}$), we must minimize $I_U$ to reduce the worst-case $V_{\text{ripple}}$. Reducing $I_U$, however, requires increasing the $N_{\text{PWR}}$ for the same target $I_{\text{LOAD}}$. This worsens the dynamic load regulation performance as the controller is forced to work in a larger search space. Existing works aimed to reduce $V_{\text{ripple}}$ through large $N_{\text{PWR}}$, unit power-FET toggling [47, 48], and analog ripple control module [49], but they had to sacrifice dynamic load regulation performance and consume large power overhead.

In this chapter, we propose mainly two techniques to improve the PSRR and $V_{\text{ripple}}$ problems, and achieve fast dynamic load regulation simultaneously. First, for PSRR, we implement a power-FET array comprising of $V_{\text{IN}}$-insensitive NMOS current sources that are digitally switchable through PMOS headers. In the proposed power-FET configuration, we also compensate for the temperature sensitivity by biasing the gate of the NMOSs with an on-chip complementary-to-absolute-temperature voltage ($V_{\text{CTAT}}$) reference. Second, for $V_{\text{ripple}}$ reduction, we design the LDO with small $I_U$ ($\approx 6$ nA), yet large $N_{\text{PWR}}$ (11 bits). Then, we augment the TD digital feedback controller with ED initialization control for fast load regulation. We prototyped a 10-$\mu$A-class digital LDO employing the above techniques in a 65nm low-power (LP) process. Measurements show that the chip achieves (i) high PSRR of -32dB at 1MHz with a small $I_Q$ of 125.8nA, (ii) a nominal (worst-case) $V_{\text{ripple}}$ of 2.6mV (10.9mV), (iii) output voltage stability of
Figure 4.2: (a) Power-FET current variations across $V_{IN}$ and (b) voltage ripple across load currents and temperatures.

58.1 ppm/$^\circ$C, and (iv) the dynamic load regulation pF-FoM of 0.085pF.

4.2 Proposed power-FET configuration

The proposed power-FET configuration is shown in Figure 4.1 (b). For generating the $V_{IN}$-insensitive current, the NMOS current source can be biased either in the sub- or super-threshold ($V_{TH}$) region. In the sub-$V_{TH}$ regime, it achieves small $I_{PWR}$ variability (0.14%/mV) at a small $V_{DROPOUT}$ of 100mV ($\approx$3–4-thermal voltage ($V_T$)). This is more than $10 \times$ smaller variability compared to the conventional linear biased PFET (Figure 4.2 (a)). For the case of the super-$V_{TH}$ regime, we can further reduce the $I_{PWR}$ variability down to 0.04%/mV, but this requires a larger $V_{DROPOUT}$ of $\approx$300mV to be biased in saturation. The proposed power-FET configuration with $V_{IN}$-insensitive current can largely improve the LDO’s PSRR performance.

As we target the loads in a sub-mW SoC, the sub-$V_{TH}$ biased power-FET is beneficial for achieving small $V_{DROPOUT}$ and small $I_U$ ($\approx$6nA). While the sub-$V_{TH}$ biased NMOS power-FET takes up more area than the conventional linear PMOS power-FET, it is still not dominating
(5.2%) as compared to the $C_{OUT}$ (32.8%) and the rest of the circuitry. Additionally, sub-$V_{TH}$ saturated power-FETs can achieve smaller $V_{ripple}$ than linear power-FETs because of the larger transconductance ($g_m$) at the same $I_{LOAD}$ and temperature (Figure 4.2 (b)).

### 4.3 Overall digital LDO architecture

![Architecture of the proposed digital LDO.](image)

The overall architecture of the proposed LDO is shown in Figure 4.3. It comprises of four main building blocks: (i) the comparators to sample the $V_{OUT}$ (one DT comparator for the $V_{SP}$ and two CT comparators for the undershoot/overshoot detection), (ii) the TD digital integral controller, (iii) the ED initialization controller, and (iv) an 11-bit current-source based NMOS power-FET array with a $V_{CTAT}$ generator.

### 4.4 Voltage reference design and $I_{PWR}$ temperature compensation

As discussed in section 4.2, the $I_{PWR}$ of the proposed sub-$V_{TH}$ power-FET array is insensitive to $V_{IN}$; however, it can still vary exponentially with temperature. Therefore, we investigate to reduce the $I_{PWR}$’s temperature sensitivity. To do so, we bias the gate of the NMOS power-FETs with $V_{CTAT}$. This $V_{CTAT}$ is generated by an embedded on-chip $V_{CTAT}$ generator as shown in Figure 4.4. The $V_{CTAT}$ generator comprises of two parts: (i) a cross-coupled charge
Figure 4.4: Schematic of the $V_{CTAT}$ generator with a charge pump (left) and $V_{CTAT}$ core.

Figure 4.5: $V_{CTAT}$ PSRR performances across frequencies and $C_G$s.

pump (left) and (ii) a voltage generation CTAT core (right). The charge-pump generates the $2 \cdot V_{IN}$ supply for the CTAT core using an internal current-starved oscillator ($CLK_{CP}$) operating at 35kHz. The $V_{CTAT}$ generation core is designed based on the 2T voltage reference [50]. Since the core consumes only tens of nW power, the charge pump only requires using small flying and decoupling capacitors of $C_{P0}=C_{P1}=5pF$ and $C_L=10pF$. In this design, the $2 \cdot V_{IN}$ domain is


supported from \( V_{IN} = 0.5 \text{V} \) to 1\( \text{V} \) without voltage compliance issues. As shown in Figure 4.5, the \( V_{CTAT} \) generator achieves up to -40dB PSRR with the 20pF on-chip output capacitor \( (C_G) \).

4.5 Digital controller architecture

The proposed digital controller including the TD integral controller and ED initialization controller is shown in Figure 4.6. In the TD integral controller (Figure 4.6 right), we implement a slow clock \( (CLK_{LDO} = 30\text{kHz}) \) to minimize the \( \alpha \) term in Figure 4.1 (b) as to reduce \( V_{ripple} \) [12]. Since the 30kHz controller has a long feedback latency (\( \sim 33\mu\text{s} \)), however, it results in poor \( V_{DROOP} \) and \( T_S \) performances. To address this, we augment the TD controller with an ED initialization control to immediately recover a large \( V_{DROOP} \) event. The ED initialization operates based on a 7-bit time-to-digital converter (TDC), which reduces the controller’s search space from \( 2^{N_{PWR}} (=2^{11}) \) to \( 2^{N_{PWR} - N_{TDC}} (=2^4) \), where \( N_{TDC} \) (7 bit) is the bit count of the TDC. This proposed control takes similar search cycles with the SAR search [6] in the worst case (16 vs. 11 cycles for \( N_{PWR} = 11 \)), but can require fewer cycles in nominal cases.

A timing diagram of the proposed controller’s operation is shown in Figure 4.7. The ED initialization operates as follows. Immediately after the lower (upper) CT comparator detects \( V_{OUT} \) crossing the reference level \( V_{CT[0]} = V_{SP} - 5\text{mV} \) (\( V_{CT[1]} = V_{SP} + 5\text{mV} \)), it triggers the TDC by enabling an embedded oscillator (100MHz at 0.55V) for the 7-b counter (Figure 4.6 left). The generated clock, \( CLK_{TDC} \), also enables one of the DT comparators inside the stop counter. For the case of \( V_{DROOP} \), once the lower DT comparator detects \( V_{OUT} \) crossing the reference level, \( V_{CT[0]} - \Delta V \), it stops the oscillator and the counting. Here, the counter value (\( CNT[6:0] \)) represents the time (\( \Delta t \)) that \( V_{OUT} \) drops by \( \Delta V \). Therefore, for a chosen \( \Delta V \) (=30mV), we can estimate the amount of extra power-FET current required, or the digital code (Error[11:0])
Figure 4.6: Architecture of the proposed TD integral controller with ED initialization control.

Figure 4.7: Timing diagram of the proposed controller operation.

needed to be added to the output of the integral controller, D[10:0], to immediately recover the $V_{DROOP}$. This initialization process is performed through an ED pulse (marked as ED_pulse in I_CLK of Figure 4.7) to instantly update D[10:0]. After this process, the controller switches back to the TD integral control.
4.6 Measurement results

Figure 4.8: Chip micrograph and the area breakdown.

<table>
<thead>
<tr>
<th>Modules</th>
<th>Area [mm²]</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparators</td>
<td>0.00183</td>
<td>5.0</td>
</tr>
<tr>
<td>Digital controller</td>
<td>0.00703</td>
<td>19.2</td>
</tr>
<tr>
<td>Power-FETs</td>
<td>0.0019</td>
<td>5.2</td>
</tr>
<tr>
<td>CTAT core</td>
<td>0.0062</td>
<td>17.0</td>
</tr>
<tr>
<td>Charge pump</td>
<td>0.0009</td>
<td>2.4</td>
</tr>
<tr>
<td>C_P0, C_P1, C_L (total 20pF)</td>
<td>0.0029</td>
<td>8.0</td>
</tr>
<tr>
<td>C_O (20pF)</td>
<td>0.0038</td>
<td>10.4</td>
</tr>
<tr>
<td>C_O (50pF)</td>
<td>0.012</td>
<td>32.8</td>
</tr>
<tr>
<td>Active area</td>
<td>0.018</td>
<td>48.7</td>
</tr>
<tr>
<td>Total area</td>
<td>0.037</td>
<td>100</td>
</tr>
</tbody>
</table>

Figure 4.9: Waveform showing LDO’s PSRR performance for $V_{OUT}$.

Figure 4.8 shows the micrograph and area breakdown of the prototyped chip in a 65nm LP process. Measurements show that the proposed LDO achieves good PSRR performance of -25 ~ -32dB across 1k to 10MHz frequency only with an on-chip 50pF $C_{OUT}$ (Figure 4.9 and Figure 4.10). It also achieves small $V_{ripple}$s across $I_{LOAD}$s and temperatures (Figure 4.11). $V_{ripple}$ is
Figure 4.10: $V_{\text{out}}$ PSRR performance across frequencies and $C_{\text{OUTs}}$.

Figure 4.11: $V_{\text{ripple}}$ measurement across $I_{\text{LOADs}}$ and temperatures.

measured to be 2.6mV in the nominal condition of 24°C and 8.7μA $I_{\text{LOAD}}$. In the worst-case condition of 80°C and 31nA $I_{\text{LOAD}}$ (temperature$_{\text{max}}$ and $I_{\text{LOAD,min}}$), $V_{\text{ripple}}$ is 10.9mV. The $V_{\text{CTAT}}$ compensates the $V_{\text{ripple}}$ at high temperature corners, reducing the worst-case $V_{\text{ripple}}$ by 1.8× as compared to the non-temperature compensated baseline. Figure 4.12 shows that the LDO achieves accurate $V_{\text{OUTS}}$ across temperatures with a temperature coefficient (TC) of 58.1 ppm/°C.
Figure 4.12: $V_{OUT}$ and $V_{CTAT}$ measurements across temperatures.

Figure 4.13 shows the measured dynamic load regulation performances. For a $\Delta I_{LOAD}$ of 8.25µA/0.1ns, the LDO exhibits good $V_{DROOP}$ performance of 50mV ($\approx$11% of $V_{OUT}$) and $T_S$ of 3.4µs. The proposed initialization control reduces $V_{DROOP}$ up to 7.5× and $T_S$ up to four orders of magnitude over the TD integral-control-only baseline (Figure 4.14). Figure 4.15 shows the LDO’s current and power efficiency performances. At 0.55V (1V) $V_{IN}$, the proposed LDO consumes a small $I_Q$ of 125.8nA (266.0nA), achieving a peak current efficiency of 98.7% (98.3%) and a peak power efficiency (PCE) of 80.8% (88.5%) with $V_{DROPOUT}$=100mV. While this work focused on implementing the sub-$V_{TH}$ biased power-FETs for sub-mW SoCs, the proposed LDO can also be configured to have the power-FETs saturated in the super-$V_{TH}$ regime for targeting larger $I_{LOADs}$ (>1mA). However, we have to trade off with larger $V_{DROPOUT}$ (300mV) and lower PCE.
Figure 4.13: Load transient response of the proposed LDO with ED initialization vs. TD integral-control-only baseline LDO.

Figure 4.14: Measured $V_{DROOP}$ and $T_s$ performances across $\Delta I_{LOAD}$ for proposed LDO with ED initialization vs. TD integral-control-only baseline LDO.
Figure 4.15: Measured (a) current and (b) power efficiencies across various $V_{IN}$ and $V_{OUT}$ conditions.

4.7 Comparison against prior art

Lastly, we compare our work to the state-of-the-art digital LDOs targeting PSRR or $V_{\text{ripple}}$ improvement (Table 4.1). A prior work [45] can achieve $\sim -12 \text{ to } -42 \text{ dB} \text{ PSRR}$, but for high PSRR it requires using mostly only analog LDO tiles operating above 1V $V_{IN}$, thereby consuming a large $I_Q$ of 6.370nA. In comparison, the proposed LDO achieves $\sim -25 \text{ to } -32 \text{ dB} \text{ PSRR}$ at 0.55V $V_{IN}$ with more than 50x smaller $I_Q$. [47] and [48] report $V_{ripple}$ of 2mV and 6mV in the nominal conditions, but they do not report the worst-case $V_{ripple}$ conditions. For dynamic load regulation, we compute the pF-FoM (FoM1). However, since the pF-FoM is a strong function of the $T_{\text{EDGE}}$, we normalize it to the reported $T_{\text{EDGE}}$ in FoM2. Our design achieves the best FoM of 0.0085pF among the designs reporting sub-0.6V $V_{IN}$ [46 - 48].
Table 4.1: Comparison against prior works targeting PSRR or \( V_{\text{ripple}} \) improvements.

<table>
<thead>
<tr>
<th>[45] ISSCC'19 ( ^{1} )</th>
<th>[46] CICC'19</th>
<th>[47] ISSCC'19</th>
<th>[48] ISSCC'18</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design parameters</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process</td>
<td>14nm</td>
<td>65nm</td>
<td>65nm</td>
<td>40nm</td>
</tr>
<tr>
<td>Type</td>
<td>Analog+Digital</td>
<td>Analog+Digital</td>
<td>Digital</td>
<td>Digital</td>
</tr>
<tr>
<td>Power-FET</td>
<td>PMOS, Linear</td>
<td>PMOS, Linear</td>
<td>PMOS, Linear</td>
<td>PMOS, Linear</td>
</tr>
<tr>
<td>( V_{\text{DROP}} ) [mV]</td>
<td>300-350</td>
<td>50-100</td>
<td>50-100</td>
<td>100</td>
</tr>
<tr>
<td>( V_{\text{IN}} ) [V]</td>
<td>1-1.2</td>
<td>0.5-1.2</td>
<td>0.5-1</td>
<td>0.6-1.1</td>
</tr>
<tr>
<td>( V_{\text{OUT}} ) [V]</td>
<td>0.7-0.85</td>
<td>0.45-1.15</td>
<td>0.4-0.95</td>
<td>0.5-1</td>
</tr>
<tr>
<td>( C_{\text{OUT}} ) [pF]</td>
<td>200</td>
<td>20</td>
<td>100,000 (off-chip)</td>
<td>4,700 (off-chip)</td>
</tr>
<tr>
<td>Total area [mm(^2)]</td>
<td>0.024</td>
<td>0.04</td>
<td>0.048 *</td>
<td>0.18 **</td>
</tr>
<tr>
<td><strong>Dynamic load regulation performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{DROOP}} ) [mV] @ ( I_{\text{LOAD}} )</td>
<td>83 @ 15mA</td>
<td>65 @ 10mA</td>
<td>38 @ 9.5( \mu )A</td>
<td>40 @ 19mA</td>
</tr>
<tr>
<td>( T_{\text{EDGE}} ) [ns]</td>
<td>&lt;0.015</td>
<td>5</td>
<td>&lt;500</td>
<td>400</td>
</tr>
<tr>
<td>FoM1 [pF] (^{1})</td>
<td>0.010</td>
<td>0.007</td>
<td>0.66</td>
<td>0.39</td>
</tr>
<tr>
<td>FoM2 [pF] (^{2})</td>
<td>0.00015</td>
<td>0.035</td>
<td>330</td>
<td>156</td>
</tr>
<tr>
<td><strong>Accuracy &amp; efficiency performance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IN}} ) [V]</td>
<td>1.1</td>
<td>0.6</td>
<td>0.5</td>
<td>0.6</td>
</tr>
<tr>
<td>( I_{\text{D}} ) [mA] (^{3})</td>
<td>6.370</td>
<td>29,000</td>
<td>0.745</td>
<td>19,600</td>
</tr>
<tr>
<td>( I_{\text{LOAD, min}} )</td>
<td>N.R.</td>
<td>0A</td>
<td>710( p )A</td>
<td>N.R.</td>
</tr>
<tr>
<td>( I_{\text{LOAD, max}} )</td>
<td>15mA</td>
<td>12mA</td>
<td>270( \mu )A</td>
<td>20mA</td>
</tr>
<tr>
<td>Peak PCE nominal [%]</td>
<td>77.3</td>
<td>83.1</td>
<td>90.0</td>
<td>83.3</td>
</tr>
<tr>
<td>Peak PCE @ ( V_{\text{OUT}}=0.45)V [%] (^{4})</td>
<td>40.9</td>
<td>74.8</td>
<td>90.0</td>
<td>75.0</td>
</tr>
<tr>
<td>( V_{\text{ripple, nominal}} ) [mV]</td>
<td>0**</td>
<td>0**</td>
<td>2@710( p )A (N.R.)</td>
<td>6@20mA (27°C)</td>
</tr>
<tr>
<td>( V_{\text{ripple, worst case}} ) [mV] (^{3})</td>
<td>N.R.</td>
<td>N.R.</td>
<td>N.R.</td>
<td>N.R.</td>
</tr>
<tr>
<td>( V_{\text{OUT}} ) TC [ppm/°C]</td>
<td>N.R.</td>
<td>N.R.</td>
<td>N.R.</td>
<td>N.R.</td>
</tr>
<tr>
<td>PSRR [dB]</td>
<td>-2 to -18 ***</td>
<td>-2.5 * to -22</td>
<td>(100kHz–10MHz)</td>
<td>N.R.</td>
</tr>
<tr>
<td>@1kHz–10MHz</td>
<td>-12 to -42 ****</td>
<td>(100kHz–10MHz)</td>
<td>N.R.</td>
<td>N.R.</td>
</tr>
</tbody>
</table>

\( ^{1}\)Computed from FoM and current efficiency plot if range was reported.  
\( ^{2}\)FoM2 = \( (I_{D}/I_{\text{LOAD}}) \cdot (\Delta V_{\text{OUT}}/V_{\text{IN}}) \cdot C_{\text{OUT}}/I_{\text{LOAD}} \) \( \mu \)s.  
\( ^{3}\)Estimated based on \( I_{D} \) and \( I_{\text{LOAD}} \) if PCE @ \( V_{\text{OUT}}=0.45\)V is not reported.  
\( ^{4}\)Reported for the high PSRR version.  

**N.R. = Not Reported**

---

\( ^{1}\)Computed from FoM and current efficiency plot if range was reported.  
\( ^{2}\)FoM2 = \( (I_{D}/I_{\text{LOAD}}) \cdot (\Delta V_{\text{OUT}}/V_{\text{IN}}) \cdot C_{\text{OUT}}/I_{\text{LOAD}} \) \( \mu \)s.  
\( ^{3}\)Estimated based on \( I_{D} \) and \( I_{\text{LOAD}} \) if PCE @ \( V_{\text{OUT}}=0.45\)V is not reported.  
\( ^{4}\)Reported for the high PSRR version.  

**No ripple when Analog loop dominates.**

***Reported for 1x Analog + 15x Digital LDO configuration.**

*****Reported for 28x Analog LDO configuration.**
4.8 Summary

In this chapter, we designed a fully-integrated digital LDO aimed for a sub-mW SoC. To do so, we proposed an LDO with very small power overhead ($I_Q = 125.8\text{nA}$), yet with fast dynamic load regulation. Additionally, we tackled the classical PSRR and $V_{\text{ripple}}$ problems of a digital LDO. Thanks to the proposed $V_{\text{IN}}$-insensitive and temperature-compensated NMOS current-source based power-FET array configuration, the design achieves excellent PSRR of -25db ~ -32dB and nominal (worst-case) $V_{\text{ripple}}$ of 2.6mV (10.9mV). Also, we implemented an ED initialization control in the TD integral controller, achieving significant improvements in the dynamic load regulation performances.

Recently, integrated LDOs were used to protect hardware encryption cores against side-channel attacks (SCAs). Integrated LDOs are promising for such applications as they not only isolate the measurement node of the load circuit (which is attacked by a hacker) from an off-chip supply, but also provide fast load regulation. However, security resilient LDOs incur considerable performance, power, and area overheads. This chapter presents EQZ-LDO, a digital LDO with shunt-resistor detection and on-demand current equalization for SCA resistance. The goal is to amortize the LDO's energy-delay-product (EDP) overhead over the lifetime of a device through a detection-driven activation scheme. We prototyped a chip in a 65nm CMOS process. The proposed design incurs 0.5% power overhead and 0% performance degradation, scaling the EDP overhead down to 1.005×. We performed the correlation power attack (CPA) on an AES core protected by EQZ-LDO for more than 7.5M traces and the secret key has not yet been disclosed.

5.1 Motivation

Hardware cryptographic engines, such as an AES core, leak side-channel information (i.e. delay or power consumption) that can be easily exploited by a hacker to disclose the internal secret key. This is especially a problem for IoT devices as it becomes increasingly easier to gain physical access. Therefore, it is critical to enable sufficient resiliency against SCAs for these hardware encryption devices.
However, high security resiliency comes at a high performance and energy price tag. For instance, a prior work [51] has proposed a switched-capacitor current equalizer (EQZ) (Figure 5.1, left), which can equalize the supply current draw through isolated on-chip capacitors. It achieved a high MTD of >10M samples for the CPA on a 128b AES core. However, the design required the EQZ to be active during every encryption operation. As shown in Figure 5.2, this incurs a large energy-delay-product (EDP) overhead of 5.3×. As the average attack rate ($\alpha_{\text{attack}}$) is typically very low during the total lifespan of a device, such an active-for-all-rounds architecture inevitably leads to substantial energy waste when the encryption core is not under attack.

Another work [52] proposed an active-for-some-rounds EQZ (Figure 5.1, middle) to reduce the energy overhead. It enabled the EQZ only at the first and last rounds of the AES encryption process, which are commonly targeted by a hacker. Nonetheless, it only marginally improves the energy overhead (Figure 5.2). Also, it leaves the other rounds unprotected against the SCA. Other works have implemented shunt linear regulators [53, 54] and integrated regulators with control loop randomizers [4, 5, 55, 56] for improving the SCA resistance. But still, these countermeasures are based on the active-for-all-rounds architecture and suffer from a less but similar EDP overhead challenge.

In this chapter, we aim to achieve a near-zero EDP overhead with high SCA resiliency. To do so, we introduce a detection-driven paradigm. The key is to have the device be able to detect a hackers’ attack attempt and only if it detects, enable the SCA countermeasure. This paradigm allows employing very strong (generally power-hungry) mitigation schemes (i.e. current equalizer), yet exercise them only when needed. Therefore, it can amortize the EDP overhead over the lifetime of an IoT device.
Figure 5. 1: Operation of prior active-for-all/some-rounds current equalizer vs. proposed detection-driven activation based current equalizer.

Figure 5. 2: Performance comparison of energy-delay-product (EDP) overhead vs. 1/MTD against prior works.

Based on this paradigm, we prototyped EQZ-LDO, a digital low drop-out regulator with shunt-resistor detection and on-demand current equalization (Figure 5.1, right). As shown in Figure 5.2, it incurs only 0.5% power overhead and 0% performance degradation, scaling the EDP overhead down to 1.005 × (not including the LDO voltage conversion overhead). Measurements show that the secret key has not yet been disclosed with >7.5M-trace CPA on a protected 128b AES core.
5.2 Overall architecture

The proposed EQZ-LDO architecture is shown in Figure 5.3. It has the attack detector module and the EQZ-LDO core for regulating the supply to the AES core ($VDD_{AES}$). The attack detector is enabled through the start and end signals received internally from the AES core during the encryption computation of a plaintext. An attacker performs the CPA by inserting a shunt-resistor ($R_{shunt}$) between the AES chip and an off-chip supply ($VDD_{supply}$) to capture the power traces (IR drop). Our target AES consumes only tens of μW current (up to 165× smaller as compared to the prior works, which consume mA-level current [4, 5, 51, 52, 53, 54, 55, 56, 57, 58]). Therefore, it requires to insert a relatively larger $R_{shunt}$, i.e. >15Ω, to capture average trace magnitudes of ≥1mV (≈78μA×15Ω). Hackers can also potentially perform CPA even without $R_{shunt}$ (i.e. through PCB parasitic resistance). However, it is not applicable in this design since the AES power level is too low. The attack detector aims to detect this existence of $R_{shunt}$ and if it detects, sends the protect command to the EQZ-LDO core. The circuits to detect the $R_{shunt}$ are
Figure 5.4: Timing diagram of the EQZ-LDO triggering $R_{shunt}$ detection check and switching between the EQZ mode and LDO mode.

discussed in detail in section 5.3.

The EQZ-LDO core switches to the EQZ mode if it receives $protect=1$ from the attack detector. Otherwise ($protect=0$ or AES is idle), it remains in the LDO mode. Figure 5.4 illustrates a timing diagram for this operation. Note that activating the $R_{shunt}$ check (denoted by the check_pulse signal) at every plaintext encryption consumes power and is not necessary since physically inserting $R_{shunt}$ takes time. Therefore, we target to have the attack detector perform a check sparsely over time. In our prototype, we configure the attack detector to perform the check at the beginning of an encryption operation only if it has not performed the check during the last 4ms. This checking operation is controlled through an 8-b timer.
5.3 Attack detector module

Figure 5.5 shows the detailed architecture of the attack detector. It includes a checking module (left) and an amplifier module (right). When the attack detector performs a check, the trigger generator in the checking module produces check\_pulse, which momentarily sinks a width/height-programmable check current (I\_check). If R\_shunt exists between the VDD\_supply and VDD\_on-chip, the I\_check induces a few mV of IR drop in VDD\_on-chip.

During this time, the trigger generator also enables the detection comparator to detect this drop by monitoring V\_detect, where V\_detect is the output of the amplifier module. Amplifying the IR drop into V\_detect helps to make a robust detection. The PMOS array in the amplifier core operates based on the common-gate mode and provides a voltage gain of 24dB. Its gate is biased at a subthreshold voltage (V\_sub) through an embedded 2T voltage reference (2T VR) for high g\_m. If V\_detect falls below a threshold voltage (V\_set-\Delta V), the detector considers R\_shunt added (detect=1).
Other environmental factors, such as the output ripple of an off-chip power converter, may induce a voltage drop on $V_{DD_{on-chip}}$ that causes false detection. Therefore, we aim to design the attack detector to be sensitive only to the additional $R_{shunt}$-induced voltage drop. To do so, we add a calibration block in the amplifier module, which actively sets $V_{detect}$ to $V_{set}$ over environmental $V_{DD_{on-chip}}$ variations through a slow (60kHz) digital feedback loop. During the $R_{shunt}$ checking process, this calibration loop is disabled by clock-gating ($clk_{calib}$) to properly perform the detection. This operation ensures robust detection against non-attack-induced $V_{DD_{on-chip}}$ variations.

### 5.4 EQZ-LDO core

![Architecture of the EQZ-LDO core in LDO mode.](image)

The EQZ-LDO core operating in the LDO mode ($protect=0$) is shown in Figure 5.6. It uses two CT comparators for dead zone control ($V_{SP}[1:0]$) and two DT comparators for $V_{DROOP}$ detection and compensation ($V_L[1:0]$). The controller exercises the proportional-integral (PI) control that controls two power-switch modules, A and B, with two sets of control signals for P-output1 ($S1A_{P_{out1}}$, $S1B_{P_{out1}}$), P-output0 ($S1A_{P_{out0}}$, $S1B_{P_{out0}}$), and I-output ($S1A_{I_{out}}$, $S1B_{I_{out}}$).
S1B_Iout). Yet, in the LDO mode, each control signals for A and B modules are identical. Also, each module integrates a $C_{OUT}/2$ (=30pF).

To integrate the EQZ ($protect$=1), each power switch module employs two additional switches – (i) a transmission gate (S2) and (ii) a comparator-triggered ($V_{REF,EQZ}$) shunt switch (S3). The PMOS power-FET arrays (S1) are reused as the charging switches. The 4-phase 2-cycle operation of the EQZ is shown in Figure 5.7. Its operation is as follows: (i) module-A charging; module-B supplying, (ii) module-A supplying; module-B discharging to $V_{REF,EQZ}$, (iii) module-A supplying; module-B charging, and (iv) module-A discharging to $V_{REF,EQZ}$; module-B supplying. In comparison, the prior art [51] implemented a 3-phase 3-cycle operation, which demanded three power switch modules, as well as 5× larger total $C_{OUT}$ to limit the EQZ’s switching frequency and the associated power dissipation. In this work, thanks to the detection-driven activation technique, we can greatly amortize the power overhead of the EQZ, and therefore can further scale $C_{OUT}$ by using faster switching (6.7MHz in our prototype) while ensuring no performance penalty of the AES core.
Figure 5. 7: The 4-phase 2-cycle operation of the EQZ-LDO core in EQZ mode.
5.5 Prototype and measurements

Figure 5.8: Chip micrograph.

Figure 5.8 shows the photo of our prototype chip in a 65nm process. It includes the proposed EQZ-LDO with a 128b AES core. Based on the testing setup as shown in Figure 5.9, we performed the CPA against the unprotected AES core for 10k samples (Figure 5.10 (a)). It successfully disclosed the secret key byte with a MTD of 2.5k traces. For the case of the AES protected by EQZ-LDO, we have collected so far more than 7.5M traces and the secret key byte has not yet been disclosed (Figure 5.10 (b)).

Figure 5.11 (a) shows the average magnitude of the power traces (IR drop=AES average current × R_{shunt}) in the prior and current works. In this work, we consider that the hackers can instrument IR drop as small as 1-4 mV. For our target AES, this implies that a hacker needs to insert at least 15Ω for R_{shunt} and we show that the proposed circuits can detect it as shown in Figure 5.11 (b). The proposed attack detector can also detect even smaller R_{shunt} by using a larger I_{check}. Yet, the current chip is designed to support up to 1.2mA I_{check}. 

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Figure 5.9: Testing setup to perform CPA on the AES core.

Figure 5.10: CPA against (a) unprotected AES core vs. (b) EQZ-LDO protected AES core.

Also, we measure the detection accuracy for a 30-mVpp supply noise across 100Hz-1MHz frequency in Figure 5.12. Measurements show that it achieves a 100.0% true positive with only 0.2% false positive at 100Hz and 1kHz. The false positive drops to 0.0% at higher frequencies due to the low-pass filter formed by the parasitic capacitance at the $V_{detect}$ node.
Figure 5.11: (a) Average magnitude of the AES power traces vs. average AES current against prior works and (b) shmoo plot of on-chip $I_{\text{check}}$ vs. $R_{\text{shunt}}$.

Figure 5.12: Attack detection accuracy with supply noise across frequency.
Figure 5.13: Dynamic load regulation performance of the EQZ-LDO in LDO mode.

Figure 5.13 shows the oscilloscope waveforms of the EQZ-LDO’s dynamic load transient response in LDO mode. For a $\Delta I_{LOAD}/T_{EDGE} = 386\mu A/<0.1\text{ns}$, it exhibits a $V_{DROOP} = 46.4\text{mV}$ with $C_{OUT} = 60\text{pF}$. We measure the EQZ-LDO’s current efficiency and DC load regulation performances in Figure 5.14. It achieves a peak current efficiency of 99.9% and DC load regulation of 3.37mV/mA at $V_{IN}=0.5\text{V}$.

In Figure 5.15, we plot the power overhead projection of the EQZ-LDO across the average attack rates ($\alpha_{attack}$) and the activity factors ($\alpha_{activity}$). $\alpha_{activity}$ is defined as the ratio of the AES active time over its total lifespan. For a realistic-to-pessimistic assumption of $\alpha_{attack}=1/\text{s}$-$1$/day and $\alpha_{activity}=0.0-1.0$, the EQZ-LDO exhibits only 0.5-0.9% (14.4-18.6%) power overhead not-including (including) the LDO and the voltage conversion overhead.
Figure 5. 14: Current efficiency and DC load regulation performances across $I_{LOAD}$.

Figure 5. 15: Power overhead projection of the proposed EQZ-LDO.

5.6 Comparison against prior art

Finally, in Table 5.1, we compare the proposed design with the prior works. In our design, the low-power detection circuits enable the lowest quiescent power ($P_Q$) of 650nW, which leads to the EDP overhead of only $1.005 \times (1.186 \times$ including the LDO and voltage conversion overhead). It also uses $C_{TOTAL}$ of only 60pF, marking the smallest area of $0.028 \text{mm}^2$ for the
protection circuitry. So far, the MTD for the CPA against our protected 128b AES core is $>$7.5M and increasing. Also, it is worthy to note that our proposed *detection-driven* technique can be implemented with other voltage converters or even without a converter.
Table 5.1: Performance summary and comparison against prior art.

<table>
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<td>Detection-driven activation</td>
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<td>VDD_supply [V]</td>
<td>-</td>
<td>-</td>
<td>0.6 – 1.1</td>
<td>0.65 – 1.2</td>
<td>1.1</td>
<td>0.5 – 1</td>
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<td>VDDAES [V]</td>
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<td>-</td>
<td>0.5 – 1</td>
<td>0.6 – 1.15</td>
<td>0.8</td>
<td>0.45 – 0.95</td>
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<td>99.4</td>
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<td>VDROOP @ ΔLOAD/T_EDGE</td>
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<td>-</td>
<td>235mV @ 40mA/0.1ns</td>
<td>101.7mV @ 20mA/0.1ns</td>
<td>-</td>
<td>46.4mV @ 386μA&lt;0.1ns</td>
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<td>FoM [pF]</td>
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<td>AES area [mm²]</td>
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<td>0.276</td>
<td>0.08</td>
<td>0.15</td>
<td>0.054</td>
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<td>AES power</td>
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<td>10.9mW @ 24MHz, 1.8V</td>
<td>10.9mW @ 80MHz, 0.84V</td>
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<td>C_TOTAL [pF]</td>
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<td>300</td>
<td>2300</td>
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<td>60</td>
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<td>Total area of protection circuitry [mm²]</td>
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<td>0.19</td>
<td>0.542</td>
<td>0.0223 (doesn’t include C_OUT)</td>
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<td>37.5</td>
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<td>Power overhead not including / including regulator and voltage conversion overhead [%]</td>
<td>33 / -</td>
<td>23 / -</td>
<td>- / 32</td>
<td>- / 19.4</td>
<td>- / 49.8</td>
<td>0.5 / 18.6</td>
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<td>Delay overhead [%]</td>
<td>100</td>
<td>NR</td>
<td>11.6</td>
<td>4.8</td>
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<td>0</td>
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<td>1.230b / -</td>
<td>- / 1.644</td>
<td>- / 1.310</td>
<td>- / 1.498</td>
<td>1.005 / 1.186</td>
</tr>
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<td>SCA performance</td>
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<td>MTD of unprotected AES(4)</td>
<td>4k</td>
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<td>300&lt;sup&gt;c&lt;/sup&gt;</td>
<td>500</td>
<td>8k</td>
<td>2.5k</td>
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<tr>
<td>MTD of protected AES(4)</td>
<td>&gt;10M</td>
<td>&gt;800k&lt;sup&gt;d&lt;/sup&gt;</td>
<td>800k&lt;sup&gt;c&lt;/sup&gt;</td>
<td>&gt;7M</td>
<td>&gt;1B</td>
<td>&gt;7.5M&lt;sup&gt;e&lt;/sup&gt;</td>
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<td># of measurements</td>
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<td>800k</td>
<td>10M</td>
<td>7M</td>
<td>1B</td>
<td>&gt;7.5M&lt;sup&gt;e&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

(1): Total capacitor used in the system, (2): Total area including regulator and C_OUT, (3): Quiescent power (P<sub>0</sub>) is computed based on power overhead if not reported, (4): MTD to disclose the first key byte, a: Includes regulator power, b: Does not include delay overhead, c: Observed from figures, d: Does not test unprotected intermediate encryption rounds, e: MTD is currently increasing with more measurements.

FoM = C_OUT(ΔVDDAES/VDDAES)·(LDO quiescent current/ΔILOAD), NR: Not Reported

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5.7 Summary

In this chapter, we aimed to design an integrated voltage regulator that can protect a hardware encryption engine from a hacker’s attack (SCA) with minimal overheads in power, performance, and area. To do so, we proposed EQZ-LDO, a fully-integrated digital LDO featuring detection driven on-demand current equalization for SCA resistance. Compared to the classical countermeasure circuits based on the active-for-all-rounds architecture, the proposed detection-driven scheme can greatly amortize the power overhead over time, and as a result, achieve a near-zero EDP overhead. In addition, we proposed an enhanced current equalizer circuit employing only two power switch modules to scale the $C_{OUT}$ and silicon area. In the prototype, we have so far tested more than 7.5M samples for the CPA against the protected 128b AES core and the secret key has not yet been disclosed.
Conclusion

Modern system-on-chip designs integrate microprocessors employing massively-parallel architecture with many cores, embedded memory, digital signal processing units, input/output ports, and analog/RF blocks. A low-drop-out regulator (LDO) is an attractive option to support each of these voltage domains owing to its high power density and compact design. Recently, digital LDOs became popular due to their superior low input voltage supportability for maximizing energy efficiency and process scalability as compared to their analog counterparts. However, a conventional digital LDO suffers from some key drawbacks, such as the trade-off between control loop latency and power which demands a large output capacitor, insufficient PSRR, and large output voltage ripple.

Moreover, growing computation demand over the years has led to a substantial increase in the current consumption and silicon footprint of a microprocessor core. To support such a large load, merely increasing the size of the power-FETs in the classical single LDO architecture is insufficient due to the large performance degradations caused by the non-negligible parasitics of a practical power grid.

Integrated LDOs also have started to find applications in the hardware security space. A security-aware LDO is a promising option to enhance the resistance against side-channel-attacks (SCAs) for hardware cryptographic cores. State-of-the-art SCA resilient LDO designs have shown significant improvements in securing an encryption core, however, they exhibit sizable overheads in performance, power, and area.

This thesis proposed new LDO architectures and circuit techniques to address these challenges in the modern digital LDO design. Chapter 2 proposed hybridizing the event- and time-driven control in a digital LDO for improving the dynamic load regulation performances. In
this architecture, the load event-based triggered feedforward control improves the voltage droop and the fast synchronous feedback loop shortens the settling time. Chapter 3 presented a $3 \times 3$ multiple digital LDO system based on distributed event-driven controls for supporting a large digital load. Compared to the classical single LDO architecture, the multi-LDO system achieves significant improvements in the steady-state accuracy and load transient performances. Also, compared to the prior time-driven distributed LDO designs, the proposed multi-LDO design is highly modular and can be easily expanded to an $n \times m$ matrix. The project in chapter 4 aimed to tackle the classical PSRR and output voltage ripple problems in a digital LDO. By employing a new current source-based NMOS power-FET design and event-driven initialization control, the proposed design achieved large improvements in PSRR, output ripple, and load regulation. Lastly, chapter 5 presented a SCA resilient digital LDO featuring detection-driven on-demand current equalization. The proposed detection-driven control made significant improvements in the energy-delay-product overhead compared to the prior on-chip SCA countermeasure circuits.

While this thesis presented various techniques to improve the digital LDO performances, still more research should be done to make digital LDOs more effective and reliable in commercial applications. One of the goals is to fully break the trade-off between the control loop latency and power dissipation and gear towards a highly-compact, capacitor-less design. Another objective is to further improve PSRR, but also achieve high current density and power efficiency simultaneously. Recently, efforts were made to fully synthesize the digital LDO design process to ease integration and save design time. However, to handily synthesize custom blocks such as comparators and power-FETs without performance loss remains a challenge. Lastly, techniques to improve a digital LDO’s robustness across process, voltage, and temperature variations should be further investigated.
References


