Electrostatic Modeling and Contact Resistance Engineering in 2D Semiconductor Devices

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Abstract

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The ever-increasing demand for superior devices with a smaller footprint in electronics calls for research on novel materials as a potential replacement of or integration to the existing silicon-based technology. The emergence of two-dimensional semiconductors paved a promising path in this direction. Easy isolation of atomically thin and flat layers with dangling bond free surfaces enables these materials to not only form 2D vertical heterostructures with novel properties but also facilitates advanced transistor, diode, and tunnel-device design with characteristics such as unprecedented gate-control of the channel, extremely high mobility of charge carriers, high current density, and high on-off ratios. However, like any other technology at the early development phase, 2D semiconductor research also faces numerous challenges which are needed to be addressed. In this work, we address two such challenges in the field-- modeling of vertical electrostatics in these complex novel devices which enables better understanding and prediction of their characteristics and overcoming the contact resistance issue in a promising 2D semiconductor, WSe$_2$, which enables the advancement of these devices towards near-deal characteristics.

To predict and analyze the electrical characteristics of 2D vertical heterostructures, we need to develop solid understanding of the potential landscape, charge distribution, and energy band diagrams in these devices. Conventional modeling approaches and simulation tools that have been used so far to simulate the transport characteristics obscure our intuition as the devices get more arbitrary and complex. Here, we developed a cir-
cuit equivalent model to simulate the vertical electrostatics in these novel and arbitrary heterostructures in a simple and intuitive manner. In our model, all the parameters of the energy band diagram are represented by equivalent circuit elements involving capacitors and voltage sources. We also provide an elegant approach to solve these circuits by using Gauss law in electrostatics and charge-neutrality conditions in quasi-equilibrium. With a computationally efficient algorithm developed to solve these structures, we further built an opensource tool 2dmatstack on nanohub.org that enables researchers to predict and analyze the characteristics of novel heterostructures to maximize research output.

In the next section, we focus on a major bottleneck in realizing these vertical devices experimentally. Fermi-level pinning and process-induced surface damage cause large Schottky barriers between metal contacts and these ultrathin 2D semiconducting layers resulting in large contact resistance and poor, non-ideal device performance. The solution to this problem is much more developed in the most widely studied n-type candidate, MoS$_2$, compared to the common the p-type candidate, WSe$_2$. In this work, we develop a UV-ozone-based oxidation technique that transforms the top layer of WSe$_2$ into a non-stoichiometric oxide, TOS, that degenerately dopes the layers underneath p-type. This high hole-doping decreases the Schottky barrier width at the contacts and has resulted in the lowest p-type contact resistance to ultrathin WSe$_2$ reported thus far. We show that this doping is stable in the ambient, remains active at low temperatures, repeatable, robust, and area selective for contact-doping without altering the channel properties. The high-performance ohmic contacts we demonstrate not only sets us in the path to realize near-ideal channel-dominated devices but also is pivotal to understand these devices better by eliminating the effect of contacts from the gate-controlled channel characteristics.
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Dedication

Dedicated to my mother, whose strength and support have been the biggest contributions to this milestone.
Chapter 1

Introduction

The advent of graphene in 2004 [1] opened an avenue for two-dimensional (2D) devices. Following graphene, a plethora of 2D materials of all types—metallic, semiconducting, and insulating were introduced. These materials, also known as van der Waals (vdW) materials, although have different in-plane bonding configurations, have a common property that each atomic layer is coupled to the adjacent layers by a weak vdW force. This weak out-of-plane bond allows the separation of these layers down to a monolayer precision by using techniques as simple as mechanical exfoliation using a scotch-tape [2]. The emergence of devices with atomically thin layers where the motion of electrons are naturally confined in two dimensions allows exploration of novel and fundamental phenomena in physics as well as advancements in the field of electronics and optoelectronics which were previously not attainable with three-dimensional (3D) bulk materials.

A major area of focus for 2D materials application is field-effect transistors (FET), diodes and tunnel devices. 2D semiconductors such as semiconducting transition metal dichalcogenides (TMDC) serve as the most potential candidates for the channel material in these devices. TMDCs are vdW compounds with MX$_2$ configuration, where M is a group IV to VII transition metal and X is a chalcogen atom (S, Se, or Te). Based on their
Figure 1.1: 3D Schematic of the structure of a TMDC, MoS\textsubscript{2} (left) and an FET made with a single layer MoS\textsubscript{2} as the channel (right). Image source– [3]

crystal structure and composition, these materials can be either metallic such as group V TMDCs and semiconducting such 2H phase of MoS\textsubscript{2}, WSe\textsubscript{2} and WS\textsubscript{2}. With high carrier mobility, optimum bandgap (1-2.4 eV), and single atomic-layer thickness, these materials are widely studied as a potential replacement for Si in devices.

1.1 Why 2D semiconductors for electronics

Over the past few decades, field-effect transistors made from Si have been scaling according to Moore’s law which predicted that the density of transistors on a chip would double every 2 years. However, as the transistor dimensions get smaller and channel length gets shorter, drain-induced barrier lowering, gate-induced leakage, mobility degradation, and other short channel effects become more prominent and are detrimental to the device performance. These short channel effects result in higher off-state current and thereby increasing higher static power dissipation. Mitigating these effects requires enhancing the gate control over the channel electrostatics i.e over the potential and the charge in the channel. Relation between the channel-potential and charge is given by Poisson’s equation and yields a parameter known as characteristic length, $\lambda$. In a planar
device, this length is given by $\lambda = \sqrt{t_{\text{semi}}t_{\text{ox}}(\epsilon_{\text{semi}}/\epsilon_{\text{ox}})}$, where $t_{\text{semi}}$, $t_{\text{ox}}$ are the thicknesses and $\epsilon_{\text{semi}}$ and $\epsilon_{\text{ox}}$ are the dielectric constants of the semiconductor and the gate dielectric respectively. Conventionally, the channel length is required to be much greater than $\lambda$ so that the device performance is not degraded by short channel effects. A small value of $\lambda$ can be achieved by increasing the oxide dielectric constant, reducing the gate-oxide thickness, and reducing the semiconductor body thickness. While high-k dielectrics are already being used by the industry [4], reducing the oxide thickness further than current industry standards ($\sim 1$ nm) would result in a non-uniform dielectric layer and severe gate leakage issues as charges from channel tunnel through the thin oxide. To increase the gate-channel capacitive coupling without decreasing the oxide thickness further, the industry has transitioned to gate-all-around structures known as FinFETs. However, the complex device geometry of FinFETs poses extreme fabrication challenges in pushing the technology beyond the current 7 nm node. Planar devices are much easier to fabricate compared to FinFETs and reducing the semiconductor thickness in these devices to enhance gate control is one of the promising ways to mitigate short channel effects. Although this has been achieved by ultrathin body devices such as silicon on insulator (SOI), decreasing the thickness of 3D bulk materials such as in Si is limited by the presence of dangling bonds on the surface and increased scattering of charge carriers in ultrathin samples. Creation of interface states and increased phonon coupling due to decrease in thickness in bulk semiconductors lead to significant mobility degradation detrimental to the device performance. These fundamental problems call for the investigation of novel materials that can potentially replace bulk materials in ultrathin body devices.

The absence of out-of-plane dangling bonds and thickness of less than a nanometer in monolayers of 2D semiconductors enable natural confinement of the electrons in an atomically thin 2D channel and excellent gate-coupling in an FET geometry. Encapsu-
lation of the channel in a 2D insulator used as gate dielectric such as hexagonal boron nitride (hBN) further provides atomically flat and pristine surfaces for better transport and unprecedented high mobilities (36000 cm²/V.s in MoS₂ as demonstrated by Cui et. al. [5]). With high mobility, excellent gate-controlled electrostatics, and single atomic layer thickness, 2D semiconductors are expected to provide near-ideal FET characteristics such as 60 mV/dec subthreshold swing with large on current (>1 mA/μm) and high on-off ratios (>10⁶) while still allowing further scaling of devices. Besides FETs, the ability to isolate single 2D layers and transfer them atop one another allows novel vertical structures known as vdW heterostructures with potential application for p-n junction diodes and tunnel transistors.

1.2 VdW heterostructures and their ubiquitous applications

Single or multiple layers of 2D materials can be stacked atop one another by mechanical transfer using polymer stamps to form vertical heterostructures with different crystalline orientations and different band configurations between the layers. While some of these vdW devices provide excellent platforms to study fundamental phenomena in physics such as superconductivity in twisted bilayer graphene stacked together at a specific angle known as magic angle [6], others show exciting properties suitable for device applications such as ultrafast hole transfer rate of 50 fs in MoS₂-WS₂ heterostructures [7]. The application of these vdW heterostructures in electronics is focused on novel FET design, vertical diodes, and tunnel diodes/transistors.

In one of the vertical transistor geometries, a 2D semiconductor is used as the channel material while graphene can be used for source-drain contacts [8]. Gate modulation of the work function of graphene and the Schottky-barrier height across the graphene/semiconductor interface results in a large on/off ratio that cannot be achieved in conventional
Figure 1.2: 3D schematic of vdW heterostructures for different applications. a) A vertical inverter using BSCO as p-channel and MoS\(_2\) as n-channel. b) A vertical p-n junction with stacked 2D semiconductors. Image source– [9]

planar graphene transistors. The extremely short channel (thickness of the 2D layers) also leads to high current densities. As the current and capacitance are roughly proportional to the device area, the intrinsic delay and cut-off frequency are independent of device size. This vertical geometry can be extended to 3D stacking of multiple transistors as shown by Yu et al. [8] where two graphene-based transistors with Bi\(_2\)Sr\(_2\)Co\(_2\)O\(_8\) layer as the p-channel and an MoS\(_2\) layer as the n-channel were vertically stacked demonstrating a complementary inverter with a larger-than-unity voltage gain.

Using the relatively staggered band configuration [9] of two most widely studied 2D semiconductors MoS\(_2\) and WSe\(_2\), multiple devices have been reported for tunnel diode and p-n junction applications [10, 11, 12]. For example, Nourbaksh et al. studied the transverse and lateral band-to-band tunneling in MoS\(_2\)-WSe\(_2\) heterostructures [12] and demonstrated negative differential resistance in the device. Roy et al. demonstrated a similar heterostructure with two different gates to control the p-layer and n-layer separately [11]. Although these devices exhibit rectifying behavior of typical p-n junction diodes, the fundamental mechanisms governing their behavior are different than conventional 3D devices due to the atomically thin nature of the junctions, 2D density of states (DOS), and large contact resistance issues at the metal-semiconductor interfaces. Although the elec-
Figure 1.3: Challenges in understanding vdW heterostructures. (a) The schematic of a vertical MoS$_2$–WSe$_2$ heterostructure used as a p-n junction and tunnel diode shown by Roy et al. [11]. Image source– [11] (b) Equivalent representation of the device in (a). Different 1D vertical cross-sections show different stacking arrangement, thereby making this simple p-n junction device a complex combination of multiple devices placed side by side.

The electrical properties of these 2D heterostructures have been widely studied across literature for the past few years, the fundamental difference in the electrostatics and nature of contacts preclude us from directly transferring conventional 3D device physics knowledge to analyze the electrical characteristics of these stacks.

1.3 Challenges in understanding 2D heterostructures

It took decades to understand and develop the detailed device physics in Si metal oxide FETs (MOSFET) and to optimize their geometry for superior performance and smaller footprint. Although the fundamental approaches from 3D MOSFETs can be applied to the field of 2D materials, there are novel issues that call for a detailed separate study to develop models and fabrication techniques for 2D devices.

1.3.1 Theoretical challenges

Figure 1.3(a) shows the first and the most cited vertical heterostructure made with MoS$_2$ and WSe$_2$ [11]. Here MoS$_2$ is the n-type material and WSe$_2$ is the p-type material.
On the surface, this device appears to be a simple p-n junction. However, it is more complicated than that since 2D devices are far from ideal. With the schematic presented in Figure 1.3(b), it can be observed that this p-n junction device is a combination of multiple vertical devices placed side by side. Along the cross-section $a$, the out-of-plane stacking order consists of a metal as source, an n-type semiconductor, a dielectric and a metal as the back-gate. Along $b$ the device is an n-type semiconductor, a dielectric and a metal stack. Along $c$, the heterojunction is made of a metallic top-gate, a dielectric, a p-type semiconductor, another dielectric and the metallic back-gate. The cross-section $d$ consists of a top-gate metal, a top dielectric, a p-type semiconductor and a bottom dielectric. Finally, along $e$ the device is a metal, p-type semiconductor and a dielectric heterostructure.

When used as a diode under forward bias, the current in this device should ideally be governed by tunneling-dominated interlayer Shockley–Read–Hall (SRH) and Langevin recombination between the majority carriers at the heterojunction region and can be controlled by electrostatic gating. However, the injected current here will be determined by the electrostatics below and near the source-drain regions along $a$ and $e$. Moreover, the 2D heterojunction region is not thick enough to support the depletion regions arising from initial work-function mismatch, so they extend laterally in the layers across $b$ and $d$. To understand the transport in such a complex device and to optimize the geometry, it is absolutely crucial to understand the electrostatics i.e potential and charge distribution in all of these regions. For example, Balaji et al. fabricated different gate geometries for such devices using multilayer MoS$_2$ and MoTe$_2$ and evaluated the electrostatics with both electrical characterization and ab-initio simulations [13]. However, even if we fabricate these devices, in the absence of a model and simulation methods, it will be difficult to analyze them. Although existing simulation techniques such as solving Poisson’s equation...
and non-equilibrium green’s function (NEGF) can provide some insight into the transport in these devices, it is difficult to readily adapt them to solve the electrostatics in an arbitrary vertical 2D heterostructure and thus, they do not provide an intuitive and simple understanding of the device characteristics.

1.3.2 Experimental challenges

One of the major bottlenecks in 2D device research that impacts the device performance severely is the large Schottky barrier for charge injection at the metal-semiconductor contact interface. A typical FET and other conventional devices operate entirely on the principle that the gate controls the channel electrostatics. The contacts should not be having any impact on the device characteristics and their role is limited to injecting current into the channel. Therefore, the contacts are required to be low-resistance ohmic in nature. However, the large contact resistances imposed by the Schottky-barrier make 2D semiconductor devices contact-dominated and precludes the use of the full potential of the channel. The reported on-current densities for 2D vertical heterostructure devices are much smaller (in nA range) [12, 11] compared to Si-diodes (in mA range) with similar device area and doping density. The large contact resistance not only results in small on-currents limiting the application of these devices but also poses challenges in studying the channel properties experimentally. To demonstrate the impact of the contacts further, Zhou et. al. [14] fabricated a similar geometry to Roy et. al. [11] and showed that the device characteristics arise from the modulation of Schottky-barrier at the contacts instead of the modulation at the heterojunction electrostatics.

To address this issue and fabricate superior 2D heterostructures, low resistance ohmic contacts to both n-type and p-type 2D semiconductor is required. The most widely studied n-type candidate in literature is MoS$_2$ while the potential p-type material is WSe$_2$. 
In MoS$_2$, the Fermi level is pinned near the conduction band edge leading to inherently n-type channel properties. This pinning further makes it easier to fabricate low resistance n-type ohmic-contacts. Extensive research has been performed to lower the contact resistance further in MoS$_2$ with techniques such as work-function engineering [15], interfacial layer between metal-semiconductor [16], 2D/2D contacts [17], 1T/2H contacts [18] and oxide-based doping which has led to contact resistance as low as 0.4 kΩ.μm for monolayer MoS$_2$ [19]. However, results in the same ball-park for ultrathin WSe$_2$ have not been demonstrated thus far.

To illustrate further, fig. 1.4(a) shows the transfer characteristics of a trilayer WSe$_2$ device we fabricated with Pd/Au contacts on a 285 nm thick SiO$_2$ with doped-Si as back-gate in an FET geometry. The maximum p-type and n-type drain current obtained for this device is 100 nA/μm, significantly smaller than the Si standard (1 mA/μm). Extracted contact and channel resistance with 4-probe measurement presented in fig. 1.4(b) shows that this device is completely contact dominated in all regions of gate-voltage operation with contact resistance as high as 50 MΩ.μm, more than 6 orders higher than the lowest

Figure 1.4: Contact resistance issue in 2D semiconductors. (a) Transfer characteristics of a trilayer WSe$_2$ device fabricated with standard processes with Pd/Au metal contacts. Small p-type and n-type on-currents indicate large device resistance. (b) Large channel and contact resistance extracted from the device with 4-probe measurements. 100× more contact resistance than the channel resistance at all applied gate voltages indicates an entirely contact-dominated device.
contact resistance for n-type MoS$_2$ found in the literature. With special methods for contact resistance engineering, resistance as low as 0.6 k$\Omega$.m has been achieved for bulk WSe$_2$ [20]. However, similar values for ultrathin WSe$_2$ (less than 5 nm thickness) remained a challenge thus far.

1.4 Thesis outline

This thesis is divided into two parts focused on solving two distinct but related problems in 2D device research. In chapter 2, we develop a model that allows us to understand the vertical electrostatics of vdW heterostructures. This model can calculate the potential drop, charge density, and energy band diagram across any 1D vertical cross-section of any heterostructure consisting of 2D semiconductors, metals, graphene, and dielectric-insulators stacked in any arbitrary sequence. With the intuition and understanding of the device electrostatics enabled by this theory work, we focus on solving an experimental challenge in fabricating these vertical heterostructures— large p-type contact resistance at the metal-semiconductor junction in WSe$_2$. Before discussing the technique we developed, chapter 3 provides an overview of the existing techniques for contact resistance engineering and their limitations. Chapter 4 discusses a doping method we devised to overcome the contact resistance issue in WSe$_2$ and shows the lowest p-type contact resistance achieved for ultrathin WSe$_2$ so far. Finally, chapter 5 discusses the universality of the doping technique we develop for different material systems and a potential road-map for future work.
Chapter 2

Electrostatic Modeling

To understand the electrostatic characteristics of stacks of 2D materials, it is essential to fundamentally understand the carrier density, potential drop, and energy band diagram along a vertical cross-section of the device under different applied voltages to different layers. This chapter discusses the challenges in simulating this vertical electrostatics and how we circumvent these challenges to build a simple circuit model for these devices. We explain how each term in the generic energy band diagram of a two-layer stack can be translated into respective circuit elements. We also extend this one-to-one mapping between the energy band diagram and equivalent circuit model from a two-layer vertical structure to an arbitrary $n$-layer stack consisting of 2D semiconductors, graphene, and metals separated by any dielectric or a vdW gap. Then we present an efficient algorithm to solve the circuit equation for this $n$-layer structure using Kirchoff’s voltage law, Gauss law in electrostatics, and charge neutrality at quasi-equilibrium. We further demonstrate the use of our model in simulation of experimentally demonstrated novel vdW heterostructures.
2.1 Challenges in modeling and simulation

There are two existing techniques to calculate the charge density, Fermi level, and electrostatic potential of structures made from 2D materials. Technique demonstrated by Cao et al. [21] solves the Poisson’s equation given by

$$\nabla^2 \phi = -\frac{\rho}{\epsilon}$$

(2.1)

in a 2D FET in the lateral direction, as shown in their schematic in eq. (2.1) where $\phi$ is the potential energy per unit charge, $\rho$ is the charge density and $\epsilon$ is the permittivity of the medium. In this structure, it is reasonable to assume that there is no vertical potential drop in the atomically thin 2D channel. Therefore, Poisson’s equation can be solved by placing grid points laterally along the channel and using the metallic source and drains as boundary conditions. Once the potential drop and charge density along the x-axis is determined, the current through the device can be calculated. This technique, however, cannot be directly transferred for vertical simulation on a device where multiple layers of 2D materials are stacked. The discrete nature of 2D materials makes it difficult to
place the grid points vertically to create a differential system to solve Poisson’s equation. Further, the boundary conditions are poorly defined when the structure terminates with a nonmetallic material [22].

Other techniques demonstrated by multiple groups use equivalent circuit models consisting of geometric and quantum capacitances for devices composed of a single layer or two different layers of 2D semiconductors [23, 24, 25]. However, these circuit models cannot be easily expanded to $n$ layers (as shown in fig. 2.2) since they incorporate the work function difference between the layers as a flat-band voltage shift of the gate potential [24]. A single flat-band voltage shift cannot accommodate the work function differences of an arbitrary number of layers. Similarly, their model’s definition of the voltage across the quantum capacitor does not extend to multiple layers.

Figure 2.2: An $n$-layer vdW heterostructure with voltages applied to each layer.

2.2 Quantum capacitance

In a conventional geometric capacitor consisting of two metal plates and a dielectric in between, the change in charge on the plates results in the change in electric field in the dielectric, thereby changing the potential drop across it. Metals can accommodate infinite charge without significant change to the Fermi level ($E_f$) position with respect to
the conduction band edge \( (E_c) \) and hence, do not have any voltage drop across them. The charge-voltage relationship is linear in this case and the capacitance has a simple geometric form given by, \( C_{ox} = \varepsilon A/d \) where, \( \varepsilon \) is the permittivity of the oxide, \( A \) is area and \( d \) is the oxide thickness. However, when one of the plates is replaced by a semiconductor the potential drop occurs both across the dielectric and the semiconductor. To induce any amount of charge, the \( E_c - E_f \) in the semiconductor has to change thereby giving rise to a semiconductor capacitance. For bulk semiconductors that can support a full depletion region, this capacitance can be expressed as a geometric capacitance with thickness given by the depletion layer width. Further when the plate is replaced by a 2D semiconductor and a voltage is applied, there is a potential drop across the oxide and the \( E_c - E_f \) in the semiconductor changes as we change the charge on the semiconductor. This change in charge with respect to the change in electrochemical potential is the quantum capacitance of the 2D semiconductor. However, as there is not enough thickness to support a growing depletion region when the applied voltage increases in a 2D system, the quantum capacitance cannot be expressed geometrically. Moreover, the charge-voltage relationship is non-linear in this case and can be calculated using Fermi-Dirac statistics and 2D density of states. The term quantum capacitance was first coined by Serge Luryi for a two-dimensional electron gas (2DEG) system [26].

The equivalent circuit models developed for a 2D FET such as the S2DS model by Suryavanshi et al. [24] treats the quantum capacitance in series with the oxide capacitance connected between the channel and the source. For this purpose, their definition \( E_F = qV_C \), where \( E_F \) is the Fermi level, \( q \) is unit charge and \( V_C \) is the channel potential or voltage across the quantum capacitance, works efficiently. However, in a multilayered system where all 2D layers are coupled to one another, due to simultaneous change in \( E_c - E_f \) in all layers, this definition and the series placement of quantum capacitance
with the oxide capacitance cannot be directly extended. Therefore, we redefine the quantum capacitance more intuitively for a multilayer system and derive an equivalent circuit model for the vertical electrostatics of a vdW heterostructure from the out-of-plane energy-band diagram. We show that, although the direct solution of the equivalent circuit for an \( n \)-layer structure is not possible due to the variable, nonlinear quantum capacitance of each layer, an efficient method for solving the circuit is possible using a physics-based approach consisting of Gauss law and charge neutrality condition. Overall, our model provides

(i) the ability to incorporate an arbitrary number of layers of 2D semiconductors, graphene, or metals with different work function into a vdW structure;

(ii) the ability to apply an independent potential bias to each layer;

(iii) the proper DOS for 2D semiconductors and graphene that captures the quantum effects arising from the atomic thickness;

(iv) the handling of non-degenerate and degenerate carrier concentrations through the use of Fermi-Dirac statistics; and

(v) a computationally efficient methodology that yields the energy-band diagram in the out-of-plane direction — providing a clear, intuitive picture of the charge, potential, and Fermi level across the structure.

2.3 Equivalent Circuit Model

We begin with two arbitrary layers as shown in fig. 2.3 to derive the equivalent circuit for an \( n \)-layer vdW heterostructure. The layers are either an intrinsic or doped 2D semiconductor, graphene, or metal, while the dielectric between the layers is either an
Figure 2.3: Energy-band diagrams of (a) two layers in isolation and (b) two layers in contact with one another. $E_{\text{vac}}$ is the local vacuum level, $E_c$ is the conduction-band edge, $E_f$ is the Fermi level, $W$ is the work function, $\chi$ is the electron affinity, and $V_{\text{ox}}$ is the potential drop across the dielectric. The subscript _o_ indicates parameters for a layer in isolation. (c) Equivalent circuit of the structure in (b). $C_Q$ is the quantum capacitance of a layer.

Insulator or a vdW gap [27]. Here, a vdW gap is treated as a dielectric with vacuum permittivity and atomic thickness (~5 Å). In isolation, layers 1 and 2 have different work functions, indicated by $W_{1o}$ and $W_{2o}$ in fig. 2.3(a). Once these layers are brought together in a stack, charge transfer occurs due to the work function mismatch between the layers. Figure 2.3(b) shows the out-of-plane energy-band diagram after the layers are brought together, and voltages $V_1$ and $V_2$ are applied. The potential drop across the dielectric ($V_{\text{ox}}$) can be expressed from the energy band diagram as

$$qV_{\text{ox}} = \chi_2 - \chi_1 + (E_c - E_f)_2 - (E_c - E_f)_1 + q(V_1 - V_2), \quad (2.2)$$
where \( q \) is the elementary charge, \( \chi \) is the electron affinity, \( E_c - E_f \) is the difference between the conduction-band edge and the Fermi level, and \( V \) is the applied voltage. Using the definition of work function, \( W_o = \chi + (E_c - E_f)_o \), the electron affinities can be substituted and eq. (2.2) can be rewritten as

\[
qV_{ox} = W_{2o} - W_{1o} + [(E_c - E_f)_2 - (E_c - E_f)_{2o}] \\
- [(E_c - E_f)_1 - (E_c - E_f)_{1o}] + q(V_1 - V_2),
\]

where \( W \) is the work function, and the subscript \( o \) indicates parameters for a layer in isolation. For each layer in a vdW stack, we represent the change in \( E_c - E_f \) from its value in isolation by defining a new term:

\[
qV_Q = (E_c - E_f) - (E_c - E_f)_o \tag{2.4}
\]

where \( V_Q \) is defined such that a change in \( V_Q \) induces a change in the net charge \( Q \) on a layer due to the change in \( E_c - E_f \). This represents the quantum capacitance of the layer, which is defined as

\[
C_Q = \frac{\partial Q}{\partial V_Q}. \tag{2.5}
\]

\( V_Q \) is the voltage across the quantum capacitance. We choose our definition of \( V_Q \) such that the net charge on a layer is zero when \( V_Q = 0 \) or, equivalently, when \( (E_c - E_f) = (E_c - E_f)_o \). This further implies \( V_Q \) is the channel potential. The sign of \( V_Q \) indicates the sign of the net charge on the layer. A positive \( Q \) yields a positive \( V_Q \). We can express \( C_Q \) in a more conventional form [23] in terms of the Fermi level using \(-q\partial V_Q/\partial E_f = 1\):

\[
C_Q = \frac{\partial Q}{\partial V_Q} \cdot -q\frac{\partial V_Q}{\partial E_f} = -q\frac{\partial Q}{\partial E_f}. \tag{2.6}
\]
The expression for the quantum capacitance of a layer can be found by performing the differentiation indicated in eq. (2.6) on the general expression for the net charge $Q$ in a 2D material, given by

$$Q = q(N_D^+ - N_A^- + p - n)$$

$$= q \left( N_D^+ - N_A^- + \int_{-\infty}^{E_v} g_v(E)(1 - f(E, E_f)) \, dE \right. \left. - \int_{E_c}^{\infty} g_c(E) f(E, E_f) \, dE \right)$$

(2.7)

where $N_D^+$ and $N_A^-$ are the ionized donor and acceptor concentrations per area, $n$ and $p$ are the electron and hole sheet densities, $g_c(E)$ and $g_v(E)$ are the conduction-band and valence-band DOS, and $f(E, E_f)$ is the probability that a state at energy $E$ is occupied, given a Fermi level at $E_f$. Plugging this expression for $Q$ in eq. (2.6), we have

$$C_Q = -q^2 \left( \int_{-\infty}^{E_v} g_v(E) \frac{\partial (1 - f(E, E_f))}{\partial E_f} \, dE \right.$$

$$\left. - \int_{E_c}^{\infty} g_c(E) \frac{\partial f(E, E_f)}{\partial E_f} \, dE \right).$$

(2.8)

Using Fermi-Dirac statistics, the derivative can be calculated as

$$C_Q = \frac{q^2}{kT} \left( \int_{-\infty}^{E_v} g_v(E) \frac{\exp(-\beta)}{(1 + \exp(-\beta))^2} \, dE \right. \left. + \int_{E_c}^{\infty} g_c(E) \frac{\exp(\beta)}{(1 + \exp(\beta))^2} \, dE \right),$$

(2.9)

where

$$\beta = \frac{E - E_f}{kT}.$$  

(2.10)

It is clear that $C_Q$ is a non-linear variable capacitance and its capacitance changes as a function of $V_Q$ (or, equivalently, $E_c - E_f$).
Now, with the definition of $V_Q$ in eq. (2.4), we rewrite eq. (2.3) as

\[ 0 = V_1 - \frac{W_1}{q} - V_{Q,1} - V_{ox} + V_{Q,2} + \frac{W_2}{q} - V_2, \]  

(2.11)

which represents Kirchhoff’s voltage law (KVL) for the loop shown in fig. 2.3(c). The terms $V_Q$ and $V_{ox}$ are represented by capacitances in the circuit model since these voltages are dependent on the net charge in the respective layers.

There is an initial band bending vertically across the structure due to the work function mismatch between the layers which is required to be taken into account in the circuit. The constant voltage sources equal to the work function of the layers as seen in fig. 2.3 solve this problem and obviate the need for fitting parameters to account for the initial band bending. The presence of these constant voltage sources is due to the definition of $V_Q$ in eq. (2.4). One could choose to redefine $V_Q$ such that the constant voltage offset is included as a part of the potential across the quantum capacitance; however, by doing so, the values of $V_Q$ for different layers would be shifted by the electron affinities, obscuring the physical significance of $V_Q$ since its sign would no longer be related to the net charge on the layer. Moreover, our definition of $V_Q$ highlights the flat-band condition for a multilayer structure — when the voltage applied to every layer is equal to its work function, the net charge on every layer is zero since all $V_Q$ and $V_{ox}$ are zero.

Although not shown in fig. 2.3 for the purpose of simplifying the representation, trap states can be incorporated into the model by inserting a trap capacitance in parallel with the quantum capacitance for a specific layer. The trap capacitance is the quantum capacitance due to the density of trap states with a DOS profile for $g_c(E)$ and $g_v(E)$ that corresponds to the trap distribution within the material. The provision to include trap states is useful for modeling effects such as Fermi level pinning in 2D semiconductors.

In atomically thin layers, it is reasonable to assume no potential drop across the thick-
ness of the material. However, to make our model inclusive, the vertical potential drop across a 2D layer, however small, can be incorporated into the equivalent circuit by adding a thickness-dependent geometric capacitance equal to

\[ C_{\text{geo}} = \frac{\varepsilon}{t/2}, \quad (2.12) \]

where \( \varepsilon \) is the permittivity and \( t \) is the thickness of the layer. The layer’s geometric capacitance is added in series with \( C_{\text{ox}} \), as shown in fig. 2.4. The factor of two in eq. (2.12) splits the layer’s total geometric capacitance into two halves and assumes that the layer’s charge is dependent on the potential at the vertical center of the layer. The exact calculation of the position-dependent charge in an atomically thin layer requires the self-consistent solution of the coupled Schrödinger-Poisson equations, which is not amenable to an equivalent circuit model.

Figure 2.4: The potential drop across a semiconductor layer can be incorporated into the model by defining an equivalent dielectric capacitance \( (C'_{\text{ox}}) \) that accounts for the series combination of the geometric capacitance of the adjacent layers. Here, \( C_{\text{geo}} \) is the geometric capacitance defined in eq. (2.12).

We can incorporate the vertical potential drop across the geometric capacitance of the upper and lower 2D layers by defining an effective dielectric capacitance \( (C'_{\text{ox}}) \) equal to

\[ \frac{1}{C'_{\text{ox},i}} = \frac{1}{C_{\text{ox},i}} + \frac{1}{C_{\text{geo},i}} + \frac{1}{C_{\text{geo},i+1}}, \quad (2.13) \]
as illustrated in fig. 2.4. This approach yields a linear potential profile and, hence, linear band bending vertically across the layer. Accounting for the geometric capacitance of a 2D layer is necessary when the potential drop across the 2D layer is comparable to that of the dielectric, which occurs when the 2D layer and dielectric thicknesses are similar.

\[
V_{Q,1} \quad W_{1o}/q \\
V_{ox,1} \\
V_{Q,2} \quad W_{2o}/q \\
V_{ox,2} \\
\vdots \\
V_{Q,n-1} \quad W_{(n-1)o}/q \\
V_{ox,n-1} \\
V_{Q,n} \quad W_{no}/q
\]

Figure 2.5: Equivalent circuit for an \( n \)-layer heterostructure. \( V \) is the applied voltage, \( W_o \) is the work function for the layer in isolation, \( V_Q \) is the voltage across the quantum capacitance (see eq. (2.4)), and \( V_{ox} \) is the potential drop across the dielectric.

For multilayer 2D semiconductors, a non-linear vertical potential profile arising from an inhomogeneous charge distribution can be approximated by modeling each constituent layer separately, spaced by the vDW gap. The non-linear profile (and inhomogeneous charge distribution) across a multilayer 2D semiconductor is, thus, approximated as a combination of linear potential drops (with different slopes) across the individual layers. Further, our model is developed to analyze the electrostatics in quasi-equilibrium, in the absence of charge transport. Modifications, such as using quasi-Fermi levels for electrons and holes, can be potentially incorporated to study transport phenomena in future work.
The extension of the two-layer equivalent circuit for an \( n \)-layer vdW heterostructure is shown in fig. 2.5. To solve the circuit (i.e., to determine the net charge on each layer and the potential drop across the dielectrics) for a given set of applied voltages, \( V_Q \) (or, equivalently, \( E_c - E_f \)) for each layer must be determined, yielding \( n \) unknown variables. It is important to note that if a layer is disconnected from an external bias, i.e., floating, the layer acts as a dielectric since charge is unable to flow into and out of the layer, and it (ideally) remains charge neutral.

### 2.4 Efficient Solution for an \( n \)-Layer Structure

#### 2.4.1 Derivation

The direct (naive) approach to solve the circuit presented in fig. 2.5 is to write the KVL equations for the \( n - 1 \) voltage loops. The \( n^{th} \) equation is provided by the charge neutrality condition i.e. the sum of the net charge on all the layers is equal to zero. Although, it is simple to construct these equations, the presence of \( n \) non-linear variable quantum capacitance elements, the orders of magnitude difference among the DOS of 2D semiconductors, graphene, and metals, and the lack of a closed-form expression for the charge density in graphene make the solution of these \( n \) coupled equations non-trivial. Keeping these factors in consideration, we propose an efficient solution to solve the net charge and potential drops for an \( n \)-layer vdW heterostructure.

The potential drop across the \( i^{th} \) dielectric sandwiched between \( i^{th} \) and \( (i+1)^{th} \) layer in an \( n \)-layer heterostructure can be generalized from eq. (2.2) as

\[
q V_{\alpha,i} = \chi_{i+1} - \chi_i + (E_c - E_f)_{i+1} - (E_c - E_f)_i + q (V_i - V_{i+1}).
\]  

(2.14)

In fig. 2.6, Gauss’s law is used to express the electric field of the \( i^{th} \) dielectric in terms of
charge on the preceding layers:

\[ E_i = \frac{1}{\varepsilon_{ox,i}} \sum_{k=1}^{i} Q_k. \]  

(2.15)

This allows the potential drop across the \( i^{th} \) dielectric to be expressed as

\[ V_{ox,i} = \frac{t_{ox,i}}{\varepsilon_{ox,i}} \sum_{k=1}^{i} Q_k = \frac{1}{C_{ox,i}} \sum_{k=1}^{i} Q_k. \]  

(2.16)

Here, \( t_{ox,i} \) and \( \varepsilon_{ox,i} \) are the thickness and permittivity of the \( i^{th} \) dielectric, and the summation over \( Q_k \) is the enclosed areal charge density on the preceding layers.

To find the charge density for a 2D semiconductor with parabolic bands and Fermi-Dirac statistics, eq. (2.7) can be simplified to

\[ Q = q \left( N_D^+ - N_A^- \right) 
+ g_v kT \ln \left[ 1 + \exp \left( \frac{(E_c - E_f) - E_G}{kT} \right) \right] 
- g_c kT \ln \left[ 1 + \exp \left( \frac{-(E_c - E_f)}{kT} \right) \right], \]  

(2.17)

where \( kT \) is the thermal energy, \( E_G \) is the band gap, and \( g_v \) and \( g_c \) are the constant 2D DOS for the valence band and conduction band that account for band degeneracies. For 2D semiconductors,

\[ g_{c,v} = 2 \frac{m_{c,v}^*}{\pi \hbar^2} \]  

(2.18)

where \( m_{c,v}^* \) is the effective mass for the conduction band and valence band, respectively, and \( \hbar \) is the reduced Planck constant. The initial factor of two accounts for the \( 2 \times \) valley degeneracy, common in most 2D semiconductors.
Figure 2.6: Derivation of the electric field in different dielectric layers due to the enclosed charge, based on Gauss’s law. $\mathcal{E}_i$ is the electric field, $Q_i$ is the areal charge density, and $\varepsilon_{ox,i}$ is the permittivity of the $i^{th}$ dielectric.

For graphene, the Fermi-Dirac expression for charge density can be expressed as

$$ Q = q \left( N_D^+ - N_A^- + \frac{2(kT)^2}{\pi(hv_F)^2} \times \left[ \text{Li}_2 (-\exp(-\alpha)) - \text{Li}_2 (-\exp(\alpha)) \right] \right), $$

where

$$ \alpha = \frac{E_c - E_f}{kT}, $$

$v_f$ is the Fermi velocity for graphene, and $\text{Li}_2(z)$ is the polylogarithm of order 2, also known as the dilogarithm given by

$$ \text{Li}_2(z) = \sum_{k=1}^{\infty} \frac{z^k}{k^2}, $$

which can be numerically evaluated to a desired precision using techniques provided by Crandall [28].
Now, combining eqs. (2.14) and (2.16) and rearranging the terms yields

\[
(E_c - E_f)_{i+1} = (E_c - E_f)_i + \chi_i - \chi_{i+1} + q(V_{i+1} - V_i) + \frac{1}{C_{ox,1}} \sum_{k=1}^{i} Q_k
\]  

(2.22a)

or, equivalently, in terms of work functions,

\[
W_{i+1} = W_i + q(V_{i+1} - V_i) + \frac{1}{C_{ox,1}} \sum_{k=1}^{i} Q_k,
\]  

(2.22b)

where \( W = \chi + (E_c - E_f) \). The form of eq. (2.22b) is more general since \( E_c - E_f \) is poorly defined for metal layers.

Overall, these equations suggest that once \( (E_c - E_f)_1 \) and \( Q_1 \) for the first layer are determined, \( E_c - E_f \) and, therefore, \( Q \) for all subsequent layers can be calculated iteratively, completely solving the electrostatics for the multilayer structure. Therefore, the problem of solving \( n \) equations with \( n \) unknowns reduces to determining a single unknown — the charge on the first layer. The following subsection details this algorithm.

2.4.2 Algorithm

Using the derivation from the previous section, we detail an efficient algorithm for solving the out-of-plane electrostatics of an \( n \)-layer vdW heterostructure. First, if a metal layer exists in the middle of a structure, the problem is divided into smaller sub-stacks since the metal imposes a boundary condition as detailed in fig. 2.7. Each sub-stack is solved using the following procedure:

(i) Guess \( Q_1 \). If the first layer is a 2D semiconductor or graphene, guess \( (E_c - E_f)_1 \) first and then calculate \( Q_1 \) using eq. (2.7). If the first layer is a metal, directly guess
\( Q_1 \).

(ii) Determine \((E_c - E_f)_{i+1}\) from eq. (2.22).

(iii) Calculate \(Q_{i+1}\) from \((E_c - E_f)_{i+1}\) using eq. (2.7).

(iv) Repeat steps (ii)-(iii) for subsequent layers.

(v) If the last layer is metal, determine its charge from Gauss’s law: \(Q_n = -C_{ox,n-1}V_{ox,n-1}\).

(vi) Check initial guess for \(Q_1\) by demanding charge neutrality across the sub-stack.

If \(\sum_{i=1}^{n} Q_i > 0\), go to step (i) and make the initial guess for \(Q_1\) more negative.

If \(\sum_{i=1}^{n} Q_i < 0\), go to step (i) and make the initial guess for \(Q_1\) more positive.

If \(\sum_{i=1}^{n} Q_i = 0\), the electrostatic solution has been found.

Using this algorithm, the problem of determining \(n\) unknowns for \(n\)-layers (i.e. charge on each layer) is reduced to determining a single unknown for the first layer (\(Q_1\)). Using the attained value of \(Q_1\), the remaining unknowns can be computed using eqs. (2.7), (2.16) and (2.22). Based on this algorithm, we created an open-source tool, named 2dmatstacks [29], that is freely available on nanohub.org. The MATLAB code for this tool is provided at the end of this thesis in the appendix section.

2.5 Example: Electrostatics of the Graphene-Base Hot-Electron Transistor

To validate our model, and exemplify its scope and applicability, we simulated the energy-band diagrams for different device regimes of a graphene-base hot-electron transistor (HET), experimentally demonstrated by Vaziri et al. [30]. The graphene-base HET is currently being investigated for THz applications, and a schematic of the device is shown in fig. 2.8(a). The purpose of the graphene base is to provide superior DC and RF performance over conventional HETs that suffer from carrier scattering and self-bias.
crowding in the conventional metal base. Analysis of the off-state and the on-state characteristics and optimization of this device design require the calculation of the vertical electrostatics across the multiple layers of the structure. The 2D DOS and semi-metallic nature of graphene, however, makes quantitative analysis difficult, such that only a qualitative depiction of the vertical energy-band diagram is provided in [30], as shown in fig. 2.8(a). Although quantum-mechanical simulations and ab-initio calculations for the energy bands can be performed to model the device [31], these complex techniques do not facilitate a straight-forward method that is simple to understand. For these reasons, we utilize our model to calculate the energy band diagrams of the graphene-base HET under different bias conditions, which serve as a resource to understand experimental results as well as to optimize device design.

The simulated graphene-base HET consists of an n+ Si emitter (modeled as metal with a work function equal to the electron affinity of Si), a monolayer graphene base, and a titanium (Ti) collector. The emitter-base dielectric is SiO₂ while the base-collector dielectric is Al₂O₃. The graphene is assumed to be undoped as given in [30].
Figure 2.8: (a) Device structure of the graphene-base hot-electron transistor and qualitative vertical energy-band diagrams in the off- and on-states from [30]. (b) Simulated energy-band diagram as the collector voltage is increased from 0 to 8 V. (c) Simulated energy-band diagram as the base voltage is increased from 2 to 6 V. The effective doping of graphene changes from n-type to p-type as the base voltage increases. The material parameters and dielectric thicknesses used in the simulation are from [30]; thicknesses of the emitter, base, and collector in the band-diagrams are opted for better visualization.
Figure 2.8(b) shows the off-state energy-band diagrams when all applied voltages ($V_E$, $V_B$ and $V_C$) are zero (blue) and when the collector voltage ($V_C$) is increased to 8 V (orange). All values of the electron affinities and work functions are taken from [30]. Even as the collector voltage is increased, the electrons in the emitter cannot tunnel through the large emitter-base energy barrier. Hence, the collector current is nearly zero, and the device is off. The change in the collector voltage from 0 to 8 V does not significantly change the current; however, it does change the effective doping of the graphene layer from (nearly) neutral to n-type by pulling down the Dirac point with respect to the Fermi level, as shown in the inset of fig. 2.8(b). This change in the effective doping of graphene induces a minor tilting of the energy bands of the emitter-base dielectric. Therefore, different initial doping conditions for graphene and different dielectric thicknesses will impact the energy-band diagram to varying degrees, which can be efficiently modeled with our tool.

Figure 2.8(c) shows the simulated energy-band diagrams as the base voltage ($V_B$) is increased from 2 to 6 V, with $V_E$ and $V_C$ held constant at 0 and 8 V, respectively. At $V_B = 2$ V, the emitter-base dielectric tunneling barrier is large, the tunneling probability is nearly zero, and the device remains off. At $V_B = 4$ V, the tunneling barrier is lowered. From the experimental data in [30], the device turns on sharply around 4.5 V, in reasonable agreement with what is shown by the energy-band diagrams. At $V_B = 6$ V, the dielectric barrier is lowered significantly, such that the device is strongly on.

As shown in the inset of fig. 2.8(c), the effective doping of graphene is n-type at small base voltages although it was assumed to be initially undoped. As the base voltage is increased, the Fermi level of graphene moves towards the valence band, ultimately switching the effective doping of graphene from n-type to p-type. The change in effective doping is especially important to capture since a p-n junction may develop laterally across
the graphene sheet, cutting off the base contact to graphene in the tunneling region of the device. This lateral p-n junction can be further analyzed by performing multiple 1D vertical slices as a function of lateral position across the device.

2.6 Chapter summary

In summary, we derived an intuitive equivalent circuit for vertical vdW heterostructures with arbitrary number and arrangement of 2D semiconductors, graphene, and metals. We also explained the terms in the circuit model and demonstrated their physical significance in the energy band diagram. Finally, we developed a computationally efficient method to calculate the electrostatic properties in these multilayer structures. The method reduces the $n$ unknowns of an $n$-layer stack to a single unknown, $Q_1$, for the first layer. The technique employs the proper DOS for 2D semiconductors and graphene, and can easily incorporate trap states for detailed modeling of non-ideal materials. It incorporates full Fermi-Dirac statistics allowing proper calculation of both non-degenerate and degenerate regimes of carrier densities. The method has been developed into an open-source tool, 2dmatstacks, freely available on nanohub.org.
Chapter 3

Contact Resistance in 2D Semiconductors

The quantum limit of contact resistance in semiconductors is given by \( R_{\text{C,min}} = \frac{\hbar}{2e^2k_f} \) [32] where \( \hbar \) is Planck’s constant, \( e \) is charge of an electron and \( k_f \) is Fermi wave vector. In terms of 2D carrier density this expression can be written as \( R_{\text{C,min}} = 0.026\sqrt{n_{2D}} \) [32]. With a carrier density of \( 10^{13} \text{ cm}^{-2} \), the minimum contact resistance can be calculated as 30 \( \Omega \mu\text{m} \). However, the current best experimental results are more than an order of magnitude higher than the theoretical lower limit [33]. This chapter discusses the origin of this large contact resistance in 2D semiconductors and the methods that have been developed so far to resolve the issue.

3.1 Origin of the contact resistance

Charge redistribution at the metal-semiconductor interface due to work-function mismatch creates a depletion region on the semiconductor side and an energy barrier to carrier flow across the interface as shown in fig. 3.1. Depending on the energy barrier height
and width, a contact can appear either ohmic or Schottky type. An ideal ohmic contact presents no resistance to the current flow. With a small contact resistivity, a real ohmic contact allows large current density across the contact with a small applied forward bias. For Si, such high-performance ohmic contacts display a contact resistivity, $\rho_C$, less than $10 \, \Omega \mu m^2$. Further, ohmic contacts display linear output characteristics for all applied bias range. A Schottky-type contact, on the contrary, presents a large energy barrier for the carriers, the height of which is given by Schottky-Mott rule as $\Phi_{Bn} = \Phi_{metal} - X_{semi}$ and $\Phi_{Bp} = X_{semi} + E_g - \Phi_{metal}$ where $\Phi_{Bn}$ and $\Phi_{Bp}$ are electron and hole barrier height respectively, $\Phi_{metal}$ is the metal work-function, $X_{semi}$ and $E_g$ are the electron affinity and the bandgap of the semiconductor respectively. The width of this barrier is a representation of the extent of the depletion region on the semiconductor side and thus, depends on the doping density of the semiconductor. In an intrinsic or lowly doped 2D semiconductor-metal interface, the presence of a large Schottky barrier results in a large contact resistance and limits the device performance with small current densities and non-linear output characteristics.

There are two types of charge injection mechanisms across a Schottky barrier—thermionic emission over the barrier and tunneling of charge carriers through the barrier as shown in fig. 3.1. The electron thermionic emission current over a Schottky barrier in a 2D semiconductor is given by [34]

$$ I_{thermal} = WA_{2D}^* T^{3/2} \exp\left(\frac{-q\Phi_{Bn}}{kT}\right)(1 - \exp\left(\frac{qV_D}{kT}\right)) $$  \hspace{1cm} (3.1)

where $W$ is the width of the semiconductor, $A_{2D}^*$ is the modified 2D Richardson’s constant, $T$ is the temperature, $\Phi_{Bn}$ is the electron Schottky barrier height, $k$ is the Boltzmann constant, $q$ is a unit charge and $V_D$ is the applied bias. The modified 2D Richardson’s
Figure 3.1: Carrier injection mechanisms (thermionic and tunneling) across a Schottky barrier. $\Phi_{Bn}$ is barrier height for electrons, $E_C$ is the conduction band edge and $E_F$ is the Fermi level. Green region indicates the Fermi-Dirac distribution for electrons on the metal side.

Constant can be calculated as

$$A_{2D}^* = \frac{q\sqrt{8\pi m^* k^3}}{h^2}$$  \hspace{1cm} (3.2)

where $m^*$ is the electron effective mass and $h$ is the Plank’s constant. The tunnel current across the barrier is given by [35]

$$I_{tunnel} = \frac{2q}{h} \int_{q\Psi_S}^{\Phi_{Bn}} f(E)M_{2D}(E)T_{WK}\Psi(E)dE$$  \hspace{1cm} (3.3)

where $\Psi_S$ is the semiconductor surface potential, $f(E)$ is the Fermi-Dirac distribution of the contact metal, $M_{2D}(E)$ is the number of conducting modes in the semiconducting channel given by

$$M_{2D}(E) = \frac{2\sqrt{2m^*(E - q\Psi)}}{h}$$  \hspace{1cm} (3.4)

and $T_{WK}(E)$ is the transmission probability across the barrier computed assuming a tri-
angular potential barrier using the Wentzel–Kramers–Brillouin (WKB) approximation as

\[ T_{WKB}(E) = \exp\left( -\frac{8\pi}{3h} \sqrt{2m^*(\phi_{Bn} - E)} \frac{\lambda_{SB}}{q\Psi_S} \right) \]  

(3.5)

where \( \lambda_{SB} \) represents the Schottky-barrier width.

It is evident from eq. (3.1) that a high barrier implies less thermionic current. Similarly, the wider the barrier, the lesser is the tunneling component as given by eq. (3.3) and eq. (3.5). Ideally, the Schottky barrier height can be reduced by choosing a metal with a work-function value close to the semiconductor electron affinity. However, in 2D semiconductors, this is not straightforward for multiple reasons namely– Fermi level pinning due to surface states and defects, larger bandgap for thinner layers, and alteration of surface properties of atomically thin channels during the fabrication process.

3.1.1 Fermi level pinning

Unlike conventional 3D semiconductors, the pristine surfaces in 2D semiconductors do not have out-of-plane dangling bonds and thus, do not tend to form covalent bonds with the deposited contact metal. However, 2D materials can still have surface defect states formed during growth of the material. Moreover, due to their atomically thin nature, the crystal structure of 2D semiconductors can get altered by processes involved in fabrication creating more defects. These surface defects can lead to effects such as orbital hybridization and alteration of properties of the pristine material eventually resulting in a different contact resistivity of the semiconductor underneath the metal compared to the channel [36]. If the metal strongly hybridizes with the semiconductor forming an alloy the contact resistance improves as shown in case of Ti on MoS\(_2\) [37, 38] and Pd for WSe\(_2\) [37]. However, typical thermal or e-beam metalization on 2D semiconductors leads to the formation of metal-induced interfacial states or damage-induced defects and
results in Fermi level pinning to a specific state in the middle of the bandgap [39, 40, 16]. This Fermi-level pinning is a widely known phenomenon in 2D semiconductors and extensive work has been done to investigate the origin of this pinning. One hypothesis about the origin of this pinning is the metal-induced gap states (MIGS) that arise from metal electron wave function penetrating into the semiconductor bandgap. Kerelsky et al. showed the existence of MIGS in MoS$_2$ by measuring the local density of states across the metal-semiconductor junction using scanning tunneling microscopy (STM) [41]. Another theory hypothesizes that the intrinsic defects or impurities in 2D materials are responsible for this pinning. This is supported by the observation of a high density of sulfur vacancies and metal-like impurities on MoS$_2$ using STM by Addou et al. [42]. Further, Jung et al. have demonstrated significant damage to the surface of WSe$_2$ by direct metal deposition with transmission electron microscope (TEM) studies [43]. This type of damage could be another probable cause of Fermi level pinning. Irrespective of the origin, this pinning always results in a large Schottky barrier height independent of the metal work-function used which cannot be tuned further once formed, thereby resulting in large contact resistance values.

3.2 Contact resistance engineering strategies

Over the past few years, numerous efforts have been made to reduce the contact resistance in different 2D semiconductors. All these strategies have varying impacts on different 2D semiconductors due to differences in properties as well as between bulk and thinner samples of the same material. Following are some of the widely studied techniques–
3.2.1 Work function modulation of the contact metal

Schottky-Mott rule that shows Schottky-barrier height dependence on the metal work function does not strictly apply to 2D semiconductors due to Fermi level pinning. However, tuning of the barrier height by selecting an appropriate metal has been shown for materials where the Fermi level is pinned near one of the band edges. The use of low work-function metals such as Sc has been demonstrated to improve MoS$_2$ device performance by pinning the Fermi level near the conduction band edge [44]. Density-functional theory calculations performed by Fang et al. showed a dependence of the barrier height while taking interfacial states into account [45]. With an increase in work function, this pinning gradually moves towards the middle of the bandgap resulting in a larger Schottky barrier for electrons and thereby, increasing the n-type contact resistance. However, this pinning never crosses the middle of the bandgap in MoS$_2$. This poses a larger barrier for hole transport than for electron transport, thereby making this semiconductor an inherently n-type material. This approach of contact engineering lacks generalization majorly due to thickness-dependent bandgap of 2D semiconductors and widely varying metal-semiconductor interface chemistry depending on the fabrication steps. Since the bandgap of these materials increases with decreasing layer thickness, the impact of the same metal on the contact resistance to different numbers of layers also tends to vary [46]. Typically, multilayer samples show lower contact resistance values due to a smaller bandgap. The same metal further results in different contact resistance values for different fabrication recipes such as deposition at ultra-low vacuum, different annealing temperatures and different chemical treatments [47, 48, 49]. Table 3.1 shows the issue with engineering metal work-function to make reliable contacts in MoS$_2$—the same work function metal results in different contact resistance values with different layer numbers with different fabrication recipes.
### Table 3.1: N-type contact resistance of MoS$_2$ with different metals

<table>
<thead>
<tr>
<th>metal</th>
<th>work-function (eV)</th>
<th>Number of MoS$_2$ layers</th>
<th>contact resistance (kΩ·µm)</th>
<th>special measures</th>
<th>reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>4.08</td>
<td>1</td>
<td>$10^3$</td>
<td>N/A</td>
<td>[50]</td>
</tr>
<tr>
<td>In</td>
<td>4.1</td>
<td>6</td>
<td>4.07</td>
<td>edge contact</td>
<td>[51]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>1.1</td>
<td>Low-energy deposition and substrate cooling</td>
<td>[52]</td>
</tr>
<tr>
<td>Ti</td>
<td>4.3</td>
<td>2</td>
<td>30</td>
<td>annealing</td>
<td>[48]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9</td>
<td>0.5</td>
<td>selective etching and 12 hour annealing</td>
<td>[49]</td>
</tr>
<tr>
<td>Ni</td>
<td>5.0</td>
<td>7</td>
<td>4.2</td>
<td>N/A</td>
<td>[15]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>1.8</td>
<td>hBN tunnel layer</td>
<td>[53]</td>
</tr>
<tr>
<td>Au</td>
<td>5.2</td>
<td>9</td>
<td>4.5</td>
<td>N/A</td>
<td>[15]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>0.7</td>
<td>ultra-high vacuum deposition</td>
<td>[47]</td>
</tr>
</tbody>
</table>

Contact resistance engineering by selecting appropriate metals becomes more difficult in 2D semiconductors where Fermi level is often pinned to the middle of the bandgap such as in WSe$_2$ [54]. In spite of their similar work function, Ni contacts result in n-type transport in WSe$_2$ while Pd contacts make it p-type [54]. Similarly, the Fermi level in Al is closer to the conduction band edge of the WSe$_2$ than that in Ag. So, Al is expected to form better n-type contacts to WSe$_2$ than Ag. However, the absence of d-orbital in Al leads to low electron density at the metal-semiconductor interface resulting in poor contacts, whereas strong d-orbital overlap of Ag with WSe$_2$ results in better n-type contacts than Al [55]. This unreliable nature of work-function engineering for contacts in 2D semiconductors has motivated researchers to investigate more effective strategies to improve contact resistance.
3.2.2 Edge contacts

In 2013, Wang et al. have demonstrated the lowest contact resistance to graphene by using one-dimensional edge contacts as shown in figure [56]. A bottom-down approach was used to fabricate the edge contacts where the graphene was covered with hBN followed by etching of patterned areas to deposit metal that is contacted at the edge of graphene. This approach has yielded good quality contacts to multilayer MoS$_2$ as shown by Yang et al. by unpinning the Fermi level [57]. The presence of dangling bonds at the edges of 2D semiconductors allows greater orbital overlap enabling low resistance contacts with this method. However, the difficulty in optimizing the etch rate poses challenges in making physical contacts to ultrathin 2D semiconductor layers with a top-down approach.

A bottom-up approach was demonstrated for WSe$_2$ where monolayers were grown with chemical vapor deposition (CVD) from the edges of pre-defined Pt/Ti seeds [58]. However, this method resulted in poor quality of the channel material (low mobility values) and with the use of ionic liquid gating, the best contact resistance achieved was 16 k$\Omega$.\mu m which is still much higher than what we present in our work in the next chapter. Moreover, the intricate nature of edge contact fabrication involving multiple dry transfer steps with polymers precludes its use for large-scale fabrication.

3.2.3 Phase engineered contacts

TMDCs can occur in different polymorphic phases such as 1T (metallic octahedral), 1H or 2H (semiconducting trigonal prismatic) and 1T’ (distorted octahedral) [59]. Using n-butyl lithium treatment to form the 1T phase in MoS$_2$ as contacts to the 2H phase, Kapperla et al. were able to show excellent contacts to the material with contact resistance as low as 0.48 k$\Omega$.\mu m [18]. Since then multiple reports have been published with different
3.2.4 Interfacial layers

Numerous approaches have been adopted to resolve contact resistance issues in 2D semiconductors by trying to unpin the Fermi level at the metal-semiconductor interface. This can be achieved by inserting an interfacial layer such as an insulator or graphene at the interface. An insulator acts as a barrier to attenuate the wave function of the electron from metal to the semiconductor, thereby reducing MIGS density. Further, dipole for-
Figure 3.3: Insertion of buffer layers at metal-semiconductor interface (a) Schematic of the MoS$_2$ transistor with ZnO as an interfacial layer between Ti and MoS$_2$, taken from [16]. (b) Cross-section TEM image of the Ti/ZnO/MoS$_2$ contact (top) and conventional Ti/MoS$_2$ contact (bottom). The bottom image shows the damage caused to the few layers at the surface by direct metal deposition. Images source– [16]. (c) Schematic of the MoS$_2$ device taken from [62] showing $h$BN as an interfacial layer between MoS$_2$ and Co.

Information at the semiconductor-insulator interface is also expected to neutralize the states responsible for Fermi level pinning. By using a ZnO layer between the Ti contact and multilayer MoS$_2$, Jang et al. were able to demonstrate 0.9 kΩ.μm contact resistance [16]. Although several oxides such as MgO and TiO$_2$ have been used as the buffer layer [63, 64] the presence of dangling bonds on metal oxides and the difficulty of growing them on the 2D surface has motivated the use of atomically flat 2D insulators such as $h$BN. Cui et al. demonstrated contact resistance to MoS$_2$ as low as 4 kΩ.μm by using a single layer of $h$BN between Co-contacts and monolayer MoS$_2$ [62]. $h$BN lowers the work-function of Co due to strong lattice match and results in large interface dipoles at the interface. This eliminates the Fermi level pinning and combined with the work-function reduction, it creates an almost zero Schottky barrier between the metal and the semiconductor. Sim-
Figure 3.4: Fabrication steps in transferred via contacts method and its comparison to conventional fabrication recipe with direct deposition of metals onto the semiconductor surface.

Similar results have been demonstrated by Wang et al. for Ni-MoS$_2$ (1 kΩ·μm) [53] and by Mleczko et al. for Sc-MoTe$_2$ with bi and monolayer of hBN buffer layers [65]. While growing a thin metallic oxide as an interfacial layer is challenging, the optically transparent nature of single or bilayer of hBN makes it difficult to fabricate these devices with mechanical transfer of hBN layers. Further, with an insulator in between, the charge injection mechanism becomes purely tunneling and precludes the use of thicker buffer layers in the process as the tunnel current decreases exponentially with tunneling distance.

3.2.5 Clean interfaces and transferred contacts

Similar to an interfacial layer, a clean interface between the metal and the semiconductor where the metal is not chemically bonded to the 2D surface through hybridization allows purely tunneling contacts. In this case, the vdW gap acts as the tunnel barrier,
Figure 3.5: TVC characterization. (a) Cross-sectional TEM of a TVC shows no damage to the bilayer WSe$_2$ underneath. (b) Direct metalization causes more structural damage at multiple points of the semiconductor surface. (c) Comparison of transfer characteristics of three devices fabricated with TVC inside a glove-box, outside glove-box and with direct metalization. TVC inside a glove-box shows a much higher on-current as well as smaller subthreshold slope. (d) Transfer characteristics of the TVCs measured two months apart showing stability of the contacts.

Eliminates Fermi level pinning effects, and improves the contact resistance to the 2D channel. Based on this idea, we demonstrated p-type ohmic contacts to bilayer WSe$_2$ with a contact resistance of 7 kΩ·μm using a technique called transferred via contacts (TVC) method [43]. In this work, we fabricated metal contacts that are embedded in hBN and dry-transferred them on top of bilayer WSe$_2$ using a polymer stamp as shown in fig. 3.4. Both exfoliation of WSe$_2$ and pick-up and transfer of hBN with metal contacts were carried out in an N$_2$ glove-box environment to maintain an ultraclean 2D surface free from adsorbates.

Figure 3.5(a) and (b) shows the cross-sectional transmission electron microscope (TEM) images of the TVC device and direct-metalization contacts respectively. The direct metalization leads to damage to the bilayer WSe$_2$ at multiple points while the TVC allows a damage-free surface. Further, fig. 3.5(c) shows the transfer characteristics of devices fabricated using TVC inside glove-box, outside glove-box, and using direct metalization. A 4-order of improvement in on current and significant improvement in the subthreshold
slope demonstrates the advantages of this process over a conventional one. The stability of these contacts is demonstrated by electrical characterization of the TVC device acquired two months apart as shown in fig. 3.5(d).

We further showed that this technique can be used to fabricate top gated WSe$_2$ devices with high on-currents and near-ideal subthreshold swing of 64 mV/dec [43]. Although this technique yields high-performance ohmic contacts with ultraclean surfaces, the achieved low contact resistance is still greater than 1 kΩ.μm. Further, the intricacies of the fabrication process demand a long time for single device fabrication and are not appropriate for a scalable solution to produce multiple devices with robust contacts and high yield.

3.2.6 Doping

Thus far, all the aforementioned techniques focused on reducing the Schottky barrier height to achieve low-resistance ohmic contacts. However, in conventional 3D devices where contact resistance is an issue, decreasing the barrier width to facilitate high tunneling probability that can result in high current injection is the preferred solution. The barrier width on the semiconductor side is the depletion width which is proportional to the doping density. Therefore, heavily doping the semiconductor at the contact region results in a reduced barrier width and can enable low-resistance ohmic contacts as shown in fig. 3.6.

The conventional doping methods such as high energy ion implantation used for bulk 3D semiconductors are not applicable for 2D materials due to process-induced surface damage. Therefore novel techniques are required to be developed for ultrathin 2D surfaces. Following the substitutional doping route, it is possible to dope TMDCs during growth using appropriate precursors [66, 67, 17]. However, this method is not spatially
patternable and cannot be implemented for area selective doping of the contact region without affecting the channel. So far, the most widely studied approach has been using surface charge transfer mechanism which involves introducing the 2D surface with concentrated charges or dipoles. Different techniques have been adopted to achieve n-type and p-type surface charge transfer doping in TMDCs. These include treating the surface with a chemical such as benzyl viologen [68] for electron and AuCl$_3$ for hole-doping [34]. Yang et al. demonstrated n-type doping for few-layer MoS$_2$ using 1, 2-dichloroethane treatment and were able to attain contact resistance as low as 0.7 kΩ·μm [69]. The possible damage to the pristine channel of ultrathin devices during these chemical treatment based doping requires further. A lesser invasive and more common approach is to oxidize the 2D semiconductor surface with plasma [20] or ozone treatment [70] to form a substoichiometric oxide that dopes the semiconductor underneath due to either work-function mismatch or vacancies in the oxide which form fixed charges working as a floating gate.

Further details of such surface charge transfer based doping techniques for WSe$_2$ are discussed in the next chapter.
3.3 Contact engineering in WSe$_2$

Most of the studies found across the literature thus far focus on contact engineering specifically for MoS$_2$ compared to other TMDCs. This has resulted in high-performance n-type ohmic contacts to ultrathin MoS$_2$ with contact resistance as low as 0.4 k$\Omega$.\$\mu$m by using aluminum oxide as the dopant layer [19]. However, robust and stable ohmic contacts with resistance lower than 1 k$\Omega$.\$\mu$m to a p-type counterpart are yet to be demonstrated. As mentioned in chapter 1, the most widely studied candidate as a p-type 2D semiconductor is WSe$_2$. However, Fermi level pinning in WSe$_2$ near the bandgap along with its large bandgap in ultrathin samples ($\sim$2.1 eV in mono and bilayer) makes it challenging to attain good quality p-type ohmic contacts to ultrathin WSe$_2$. Figure 3.7 further summarizes the contact resistance of WSe$_2$ found across literature with respect to the layer number and sheet resistance. Thus far, there have been three reports of WSe$_2$ contact resistance below 1 k$\Omega$.\$\mu$m. Pang et al. show less than 1 k$\Omega$.\$\mu$m for an 8 layer WSe$_2$
device with tungsten-oxide doping by using plasma oxidation [20]. Cai et al. show similar values with molybdenum-oxide doping using rapid flame synthesis technique for 6 layer WSe$_2$ [71]. Thus far, the lowest p-type contact resistance to WSe$_2$ has been demonstrated by Chuang et al. [17]. However, it was a 10 layer device with total contact resistance of 0.6 kΩ·µm (0.3 kΩ·µm for a single contact) achieved with 30 layer Nb-doped WSe$_2$ contacts formed by substitutional doping. Moreover, the thinner devices (5 layers) showed a total resistance of 50 kΩ·µm, thereby providing room for further studies to optimize doping techniques on ultrathin devices. Resolving contact resistance issue in multilayer and ultrathin 2D semiconductors requires different approaches due to three reasons – (1) Difference in the charge injection mechanism [72]: In a multilayer device, there is a lateral path along the metal-semiconductor interface as well as a vertical path through the layers beneath for current injection. In a thin device, however, the lateral injection path dominates. Moreover, hybridization at the metal-semiconductor surface results in different resistivity of the semiconductor along the surface underneath the metal compared to the layers beneath [73]. (2) The bandgap of 2D semiconductors increases with decreasing layer thickness [46]. As the Fermi level in WSe$_2$ is typically pinned near the middle of the bandgap, metals form a larger Schottky barrier with thin devices leading to larger contact resistance than with multilayer devices. (3) The surface of the 2D semiconductor suffers from fabrication process-induced damage which affects the charge transport in ultrathin devices more than in multilayer devices [43].

The results found across the literature motivated our studies to figure out a technique that enables the formation of high-performance stable ohmic contacts with high yield and with the prospect of relatively easy and large-scale fabrication. The following chapter discusses a doping technique that we developed and optimized to achieve this goal and the corresponding results showing the best p-type contacts to ultrathin WSe$_2$ thus far.
Chapter 4

P-type Contacts to WSe$_2$

In this chapter, we address the bottleneck of large p-type contact resistance to WSe$_2$ and the method we developed to resolve it by lowering the Schottky barrier thickness at the metal-semiconductor junction using hole doping. We report the lowest contact resistance (642 $\Omega \cdot \mu$m) to sub-5 nm thin WSe$_2$ using a monolayer dopant, namely tungsten oxyselenide (TOS), that induces degenerate doping densities as high as $\sim 4 \times 10^{13}$ cm$^{-2}$. We also discuss multiple hole-doping techniques for WSe$_2$ demonstrated across the literature, none of which have been shown to be effective for ultrathin samples (less than 5 nm thick). The technique that we developed and optimized provides degenerate hole densities that remain active at low temperatures thereby enabling good quality ohmic contacts for cryogenic applications. Further, we show the stability of the doping with electrical measurements taken four months apart on TOS-WSe$_2$ devices. An important feature of our technique is the ability to selectively dope the contact regions only and we show a drastic improvement in device characteristics through area-selective doping of the contact, which opens an avenue towards achieving high-performance p-type transistors with ultra-thin 2D WSe$_2$. 

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Methods for hole doping of WSe$_2$

2D semiconductors provide a pathway to extend silicon-on-insulator technology to the atomic limit (less than 5 nm thin) which is extremely difficult to achieve with traditional epitaxial process [74], and therefore the doping methods under investigation for these materials are required to work effectively on ultrathin devices. One of the prime candidates in this family of materials is WSe$_2$. Its staggered band alignment[9] with that of MoS$_2$, an inherently n-type and widely studied 2D semiconductor, make it an ideal choice for the p-type material in 2D p-n junction diodes [11] and tunnel field-effect transistors [75]. However, the fabrication of good p-type electrical contacts to ultra-thin WSe$_2$ has been a major challenge due to Fermi level pinning at the metal-semiconductor interface giving rise to a large contact resistance irrespective of the metal work-function [76]. A potential solution for this problem is hole-doping of the semiconductor to degenerate densities at the contact region to overcome the large Schottky barrier by thinning down its width to allow hole tunneling and thereby facilitating low contact resistance. Previously reported studies have demonstrated high-performance p-type contacts for multi-layer (thicker than 5 nm) WSe$_2$ devices achieved by different hole-doping methods [17, 77, 78, 79, 80, 20]. However, for thinner channels, the band-gap increase and surface damage to the material during fabrication pose challenges in achieving good-quality ohmic contacts [43]. This calls for the development of techniques that can induce degenerate hole densities without degrading the pristine nature of these 2D surfaces in ultrathin samples.

Among previous reports, substitutional doping is a widely adopted technique for doping WSe$_2$ [17, 77, 81, 82, 78, 79]. This involves a dopant species such as niobium (Nb) introduced during chemical vapor deposition (CVD) growth of the material and requires elevated temperatures for the activation of the dopant atoms. High-temperature processing is, however, undesirable for 2D semiconductor surfaces as it is known to create de-
fects that alter the pristine channel properties [83]. The requirement of activation energy further implies that substitutionally doped contacts cannot function at cryogenic temperatures due to carrier freeze-out [84]. Methods involving chemical dopants such as terpolymer poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [85] and 4-nitrobenzenediazonium tetrafluoroborate [79] have proven effective for multi-layer WSe$_2$ samples. However, as surfaces of these materials are susceptible to degradation during chemical treatments, the applicability of doping methods involving chemicals requires further evaluation for thinner devices. Further, chemical-based and substitutional doping methods lack area selectivity implying both the channel and contact regions are exposed to equal doping. High doping density in the channel region leads to mobility degradation and poor gate-control of the device electrostatics. On the other hand, surface charge transfer mechanism [86] based techniques such as chemisorption NO$_2$ by the semiconductor [80, 87] or formation of a few-layer substoichiometric oxide at the surface using O$_2$ plasma [20, 88] or O$_3$ gas [88, 70] are proven effective for a few-layer devices and area-selective doping. While some of these processes introduce doping that is unstable with time [80] or in ambient conditions [87], others that have demonstrated stability require subjecting the material to high temperatures [70, 89] to attain degenerate hole densities. Moreover, these oxidation techniques are not self-limiting to a monolayer of WSe$_2$ and thus, lack precise control and reproducibility over the number of layers being affected in the process.

In this work, we report a room-temperature doping method using self-limiting oxidation of WSe$_2$ by O$_3$ in the presence of ultraviolet (UV) light to convert only the top layer to TOS, a non-stoichiometric oxide of tungsten (W), oxygen (O), and selenium (Se). Having precision to oxidize only a single layer reliably has not been demonstrated for WSe$_2$ in the previous studies. This monolayer TOS acts as a strong p-type dopant possibly due
to surface charge transfer facilitated by the work-function difference between the TOS and the semiconductor layers underneath[86] and has resulted in the highest hole density and the lowest contact resistance reported for sub-5 nm thin WSe$_2$ devices so far. Without any post-oxidation encapsulation, the stability of the doping in ambient conditions was observed via electrical characterizations. Measurements carried out at temperatures ranging from 300−77 K show that the degenerate densities, as well as the ohmic nature of these contacts, are retained at low temperatures. We further establish area-selectivity for our technique by covering the channel with hBN and display manifold improvement in device characteristics achieved only via contact doping without adopting measures to improve the channel.

4.1 UV ozone oxidation process

Our process involves treating WSe$_2$ in a UV-O$_3$ environment in SAMCO UV-2 system, a commercially available UV-ozone cleaning/stripping tool for 30 minutes at room temperature at an oxygen flow rate of 3L/min. The role of the UV light is to dissociate O$_3$ into molecular oxygen and highly reactive oxygen radicals that act as the oxidizing agent to form TOS.

4.1.1 Optical characterization of TOS-WSe$_2$

To confirm the formation of an oxide layer, we first performed X-ray photoelectron spectroscopy (XPS) characterization on a CVD-grown few-layer WSe$_2$ flake. The degenerate peaks in the XPS spectra before oxidation in Figure 4.1a represent W (left panel) and Se (right panel) atoms. Post-oxidation, additional convoluted peaks that appear at higher binding energies for both left and right panel in Figure 4.1b refer to the W-O and Se-O bond formation respectively [90, 91, 92]. Furthermore, the presence of degenerate W and
Figure 4.1: Material characterization (XPS and PL) of the UV-O$_3$ treatment. (a) XPS spectra of W(4f) (left) and Se(3d) (right) core level for CVD-grown few-layer WSe$_2$ before oxidation. (b) XPS spectra of the sample after oxidation showing formation of TOS with W-O bonds (left) and Se-O bonds (right). The presence of degenerate W and Se peaks both before and after oxidation indicates the presence of WSe$_2$ layers beneath. (c) The PL spectrum of the bilayer (gray) changes to a sharp monolayer peak (red) after oxidation providing evidence that only the top layer transforms to TOS. (d) Raman spectra of bilayer WSe$_2$ before (gray) and after (red) oxidation. Inset shows that the B$^{1}_{2g}$ peak disappears after oxidation corresponding to 1L WSe$_2$ with a layer of amorphous TOS on top.

Se peaks even after the process as seen in fig. 4.1b indicates minimal (if any) damage to the underlying layers. Additionally, the shift in the peaks towards lower binding energies after oxidation is indicative of p-type doping of the layers underneath [81].
Next, we confirmed the self-limiting nature of the oxidation with photoluminescence (PL) characterization on an exfoliated flake with a bilayer (2L) region (~1.4 nm thick). The broad, double-humped PL spectrum (gray) before oxidation transforms to a sharp, single peaked spectrum (red) after the process as shown in Figure 4.1c representative of the conversion of the bilayer to a monolayer. Moreover, the absence of any additional peaks in the post-oxidation PL spectrum proves that the monolayer underneath is not affected during the process. To further corroborate our claim, we performed Raman measurements on the same 2L region. In Figure 4.1d, we see similar Raman peaks ($A_{1g}/E_{2g}^1$ and $2LA(M)$) before and after oxidation signifying that the hexagonal symmetry of the crystal structure of the underlying 1L WSe$_2$ is preserved even after oxidation. The inset shows that post-oxidation the $B_{2g}^1$ peak disappears which corresponds to 1L WSe$_2$ formation with a layer of amorphous TOS on top, bolstering our claim of a monolayer dopant.

4.1.2 Atomic force microscopy (AFM) characterization

The optical microscope (OM) image, thickness determination, and surface roughness study of a trilayer (3L) WSe$_2$ flake with AFM before and after oxidation is provided in fig. 4.2. Post-oxidation optical image of the trilayer WSe$_2$ (fig. 4.2a) appears to be that of a bilayer WSe$_2$ due to the high transparency of TOS [93]. The AFM topography in fig. 4.2b shows uniform oxidation throughout, however, the surface roughness for the TOS + WSe$_2$ increases. This is expected due to the amorphous nature of the TOS. Further, the increase in the height as seen in fig. 4.2c confirms that the oxidation process is not etching the material. Different bond lengths for W-O from W-Se results in more than 1 nm increase in height in the oxidized sample compared to a non-oxidized one which is in agreement with the literature [94].
Figure 4.2: AFM characterization of the trilayer WSe\textsubscript{2}. (a) Optical microscope image of the flake before (left) and after (right) oxidation. No non-uniformity was seen optically after oxidation. (b) AFM topography shows uniform and homogenous oxidation of the entire flake with a slight increase (< 2 Å) in root mean square value of surface roughness, $R_q$, after oxidation. (c) The height maps along the A-A’ cut on the flake before (gray) and after (red) oxidation. The post-oxidation map shows more than 1 nm increase in the height after oxidation due to different bonding configurations of TOS from WSe\textsubscript{2}.

4.1.3 Structural characterization

Selected-area diffraction (SAED) pattern was used to characterize the structural properties of the TOS. The presence of SAED pattern with hexagonal symmetry along the $[0 0 0 1]$ zone axis on 1L-WSe\textsubscript{2} as seen in fig. 4.3a is indicative of the crystalline nature of the material. This diffraction pattern is completely absent in 1L-TOS which confirms the
Figure 4.3: SAED characterization of TOS (a) SAED pattern of 1L-WSe$_2$ before oxidation showing single-crystal diffraction patterns with zone axis [0 0 0 1]. (b) Post-oxidation SAED shows no pattern indicating the amorphous nature of TOS. (c) SAED patterns for two few-layer WSe$_2$ flakes before and after oxidation. The presence of a single-crystalline pattern even after UV-O$_3$ treatment establishes that the underlying layers are protected during the oxidation.

amorphous nature of TOS. However, SAED for few-layer WSe$_2$ after oxidation still shows the diffraction pattern corroborating our claim of underlying layers not getting affected in the oxidation. Further, energy-dispersive X-ray spectroscopy (EDS) was performed to find the atomic composition of the 1L-WSe$_2$ before and after oxidation. Results presented in table 4.1 show a large enhancement in the O/W ratio from before to after oxidation. However, Se is not completely removed in the process and hence, the substoichiometric oxide is termed as TOS.
Table 4.1: Atomic composition of 1L-WSe$_2$ from EDS before and after oxidation

<table>
<thead>
<tr>
<th></th>
<th>C</th>
<th>W</th>
<th>Se</th>
<th>O</th>
<th>Se/W</th>
<th>O/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pristine</td>
<td>98.87</td>
<td>0.25</td>
<td>0.72</td>
<td>0.17</td>
<td>2.88</td>
<td>0.68</td>
</tr>
<tr>
<td>Oxidized</td>
<td>94.87</td>
<td>0.55</td>
<td>0.38</td>
<td>4.2</td>
<td>0.969</td>
<td>7.64</td>
</tr>
</tbody>
</table>

Figure 4.4: AFM characterization of the WSe$_2$ used in fabricating the blanket exposure device (a) The optical microscope image of the flake after exfoliation. (b) Topography of the flake measured before etching into a hall-bar pattern. (c) Height-map shows ~2.1 nm thick flake, which is the approximated thickness for 3L WSe$_2$ [87].

4.2 Contact resistance improvement with doping

To quantify the doping and to determine its impact on contact performance, we first fabricated devices with blanket exposure to UV-O$_3$, where both the channel and edge of the contact region get oxidized. These devices enable us to characterize the hole density and the sheet resistance of the doped region and the contact resistance between the metal and the doped semiconductor with standard 4-probe measurements [95]. Figure 4.5a shows the optical microscope image of such a device which we present the following
data for. The fabrication begins with the exfoliation of a bulk WSe$_2$ crystal on a 285 nm SiO$_2$/Si$^+$ substrate. After exfoliation, a 3L flake ($\sim$2.1 nm thick) was identified with an optical microscope and the thickness was confirmed by atomic force microscopy as shown in fig. 4.4. The arbitrarily shaped flake was patterned with e-beam lithography followed by reactive ion etching, and Pd/Au (20/50 nm) electrodes were deposited to make contacts.

4.2.1 Electrical characterization of blanket exposure devices

Temperature-dependent electrical characterization of this device was then performed in a vacuum cryostat (pressure $10^{-5}$ mbar) with a bias arrangement as shown in the schematic in Figure 4.5b. Following these measurements, the device was oxidized and now the 2L WSe$_2$ + 1L TOS device was measured again in the cryostat. Figure 4.5c shows the transfer characteristics for this device before and after oxidation. The large threshold voltage shift and more than an order of magnitude change in the current (at $-100$ V of applied back-gate bias, $V_{GS}$) observed from before (gray) to after (red) oxidation indicate strong p-type doping in the latter case. Post-oxidation transfer characteristics in the applied $V_{GS}$ range appear to be that of a resistor as expected in a degenerately doped semiconductor. We determined the 2D hole density, $p_{2D}$, of the device from the transfer curve after oxidation as $3.94 \times 10^{13}$ cm$^{-2}$ at $-100$ V $V_{GS}$ and $2.87 \times 10^{13}$ cm$^{-2}$ at 0 V $V_{GS}$ using the equation $p_{2D} = I_D L_{4p} / q \mu W V_{4p}$, where $I_D$ is the current in the channel, $L_{4p}$ is the 4-probe length (between probe 2 and 3 in schematic of Figure 4.5b), $q$ is one unit of charge, $\mu$ is the field-effect mobility of the channel, $W$ is the channel width and $V_{4p}$ is the 4-probe voltage as presented in the schematic in Figure 4.5b. The field-effect mobility, $\mu$, for this device after doping was extracted as 44 cm$^2$/V.s using $\mu = (L_{4p} / C_{ox} W V_{4p}) \cdot dI_d / dV_{GS}$, where $C_{ox}$ is the geometric capacitance of 285 nm SiO$_2$. To extract the total contact resis-
Figure 4.5: Electrical characterization of a blanket-exposure device (where both the channel and contact-edge regions were exposed to UV-O$_3$ treatment). (a) Optical microscope image for the 3L WSe$_2$ device before UV-O$_3$ exposure. (b) Schematic of the device after oxidation (2L WSe$_2$ + 1L TOS) and the applied bias scheme. (c) Transfer characteristics before (3L WSe$_2$) and after oxidation (2L WSe$_2$ + 1L TOS). The large positive threshold voltage shift and increase in current after oxidation establish the formation of a highly hole-doped WSe$_2$ channel. (d) Total contact resistance (2$R_C$) and channel resistance ($R_{CH}$) of the device before (gray) and after (red) doping. Post-doping 2$R_C$ at $V_{GS} = -100$ V shows a 300× improvement.

To calculate the channel resistance, 2$R_C$, we first calculate the channel resistance, $R_{CH}$, as $R_{CH} = (V_{4p}/I_D) \cdot (L/L_{4p})$, where $L$ is the device length between the source and the drain (probes 1 and 4). 2$R_C$ is then given by 2$R_C = R_{2p} - R_{CH}$, where $R_{2p}$ is the 2-probe resistance calculated as $R_{2p} = V_{DS}/I_D$, where $V_{DS}$ is the applied drain-source bias. Figure 4.5d shows 2$R_C$ and channel resistance ($R_{CH}$) of the device before and after doping at room temperature. At the highest hole density corresponding to $V_{GS} = -100$ V, 2$R_C$ of the device was reduced from 184 kΩ·μm before doping to 0.642 kΩ·μm after doping, showing a 300× reduction.

Additionally, to verify that the improvement in sheet resistance is not arising from
Figure 4.6: Transfer characteristics of two devices before (1L-WSe$_2$) and after (1L-TOS) oxidation. It shows an n-type semiconducting behavior before doping and the current drops to the noise floor of our measurement system after doping.

To establish the reproducibility of the doping density with our process, we fabricated and characterized several 2L WSe$_2$ + 1L TOS devices repeating the aforementioned
Figure 4.7: Transfer characteristics of multiple devices before (3L WSe$_2$) and after oxidation (2L WSe$_2$ + 1L TOS). Data for device 1 is presented in fig. 4.5(c). The channel length and width for all devices are 10 $\mu$m and 4$\mu$m respectively. The variation in device characteristics before oxidation is expected for 2D semiconductors and arises during standard lithography steps. The post-oxidation positive shift in threshold voltage and increase in the on-current shows high hole doping. The variation in the current levels post-doping is due to mobility variation (44–60 cm$^2$/V.s) among the channels, however, the slopes of the transfer curves remain almost the same which indicates similar levels of doping in each device ($3–4 \times 10^{13}$ cm$^{-2}$).

scheme of fabrication. Their $2R_C$ before and after oxidation are shown in Table 4.2. The transfer characteristics of these devices before and post-doping are shown in Figure S3 of supplementary information. The post-doping $2R_C$ values in these devices remain in the range of 0.6–1.9 k$\Omega$.$\mu$m at $V_{GS} = -100$ V. While this variation can be attributed to the variation in the devices caused by standard lithography steps, the similar improvement in $2R_C$ in each device (~300×) and the calculated hole density in the range $3–4 \times 10^{13}$ cm$^{-2}$ demonstrates the repeatability of our doping method. The mobility for these devices post-oxidation varies in the range 44–60 cm$^2$/V.s. We calculate the range of sheet resistance, $R_S$, of the doped region for these devices at $V_{GS} = -100$ V using the equation $R_S = 1/p_{2DE}\mu$ as ~3.4–3.5 k$\Omega$.$\mu$m.
4.2.3 Temperature-independence of the doping

Next, measurement with varying temperature shows no degradation in the hole density as seen in Figure 4.8a. This, in turn, results in good-quality contacts preserved at low temperatures shown in Figure 4.8b. The mobility of the doped channel is expected to vary with temperature due to change in scattering. This variation results in the change of doped channel resistance with temperature and thereby changes the calculated $2R_C$ with temperature as observed in Figure 4.8b. Further, the output characteristics of the
device before and after oxidation presented in Figure 4.8c shows a shift from Schottky-type contacts (on the left) to ohmic-type contacts (on the right) both at room temperature and low temperatures. The non-linear output characteristics from before oxidation refer to current injection dominated by the Schottky-barrier at the metal-semiconductor interface. We extract the barrier height from the transfer characteristics before oxidation as $\sim 0.35$ eV. The details of the extraction method are provided in the supplementary information (Figure S4). Although the positive shift in the threshold voltage outside the range of applied $V_{GS}$ imposes a limitation on the post-doping barrier height extraction, the change observed towards linear output characteristics and an order of magnitude higher current after oxidation at all measurement temperatures in Figure 4.8d bolsters our claim of ohmic nature of the contacts. With improved contact resistance, the field-effect mobility of the device shows a reduction after doping ($44 \text{ cm}^2/\text{V.s}$) in comparison to that of the pristine channel which was found to be $202 \text{ cm}^2/\text{V.s}$ from the transfer characteristics in Figure 4.5c before UV-O3 treatment. Low mobility value in a degenerately doped semiconductor is expected due to enhanced scattering. However, this reduction in mobility at the contacts does not impair the performance when the larger channel resistance dominates the current flow through the device, which we clarify later in this chapter with a different device geometry.

4.2.4 Schottky-barrier height extraction

To confirm the Schottky-type behavior of the contacts before doping, we calculate the barrier height from the transfer characteristics of the 3L-WSe$_2$ device. The hole thermionic emission current over a Schottky barrier in a 2D semiconductor is given by[34]

$$I_{2D} = W A_{2D}^* T^{3/2} \exp\left(\frac{-q\Phi_B}{kT}\right) \left(1 - \exp\left(\frac{qV_D}{kT}\right)\right)$$  \hspace{1cm} (4.1)
Figure 4.9: Schottky barrier height extraction. (a) Transfer characteristics of the device. The dashed red line is used to find the current at flatband condition, $I_{FB}$. The $V_{GS}$ at which the transfer characteristic starts deviating from exponential subthreshold behavior is identified as the flatband voltage. The current corresponding to this $V_{GS}$ is the $I_{FB}$ (for this device ~1 nA), which we use to determine the Schottky barrier height before oxidation. (b) The tentative energy band diagram on the source side before doping. $\Phi_{Bp}$ is the Schottky barrier height, $E_F$ is the Fermi level and $E_V$ is the valence band edge. The red dashed line shows the valence band edge at flatband condition.

where $W$ is the width of the semiconductor (4 $\mu$m for our device), $A_{2D}^*$ is the modified 2D Richardson’s constant, $T$ is the temperature (300 K), $\Phi_{Bp}$ is the hole Schottky barrier height, $k$ is the Boltzmann constant, $q$ is a unit charge and $V_D$ is the applied bias (1 V for our measurements). The modified 2D Richardson can be calculated as

$$A_{2D}^* = \frac{q\sqrt{8\pi m^* k^3}}{h^2}$$  \hspace{1cm} (4.2)$$

where $m^*$ is the hole effective mass (0.44×mass of an electron for WSe$_2$)[96] and $h$ is the Planck’s constant. At the flatband condition, the tunneling current through the barrier can be assumed zero and any transport is due to the thermionic emission over the barrier. This flatband condition is signified by the point in the transfer characteristics beyond which
the current in the subthreshold region starts deviating from exponential behavior [97] (red dashed line in fig. 4.9). The current at this point is the flatband current, $I_{FB}$, which is found to be $\sim$1 nA for our device and plugging this $I_{FB}$ for $I_{2D}$ in eq. (4.1), we extract the Schottky barrier height as $\sim$0.35 eV. Such high value of the barrier height is indicative of contact dominated behavior of the device before oxidation. Post-oxidation, the shift in threshold voltage which results in the absence of the subthreshold region within the applied gate bias range precludes the extraction of the barrier height for a doped device.

4.2.5 Stability and benchmarking

Next, the stability of our doping was tested on an unencapsulated 2L WSe$_2$ + 1L TOS device kept in the ambient for four months. The transfer characteristics of this device before oxidation, just after oxidation, and after four months are shown in Figure 4.10a. The highest measured hole density for the oxidized device at $V_{GS} = -100$ V depreciated from $2.9 \times 10^{13}$ cm$^{-2}$ post-oxidation to $7.9 \times 10^{12}$ cm$^{-2}$ after four months showing only a small reduction over time. This minimal degradation can be further prevented with hexagonal boron nitride (hBN) [98] or Poly(methyl methacrylate) (PMMA) [99] encapsulation of the entire device as shown in previous works. In addition, Figure 4.10b shows our best result compared to the highest performing p-type contacts to WSe$_2$ from literature. To the best of our knowledge, total contact resistance smaller than 1 kΩ.μm has not been achieved with doping for less than 5 nm thin devices. Among the devices representing the best p-type contact resistance for WSe$_2$ reported so far, we present the lowest total contact resistance and highest hole density for thin (3L or $\sim$2.1 nm thickness) devices.
4.3 Area-selective contact doping

Having quantified the doping density and sheet resistance in blanket-exposure devices, we next fabricate a device with 3L WSe₂ and cover the channel with a patterned hBN flake shown in Figure 4.11a. Conventionally, 2D channels are encapsulated in hBN layers to facilitate clean and atomically flat interfaces with less surface defects for better transport characteristics[17]. It is necessary to ensure that the WSe₂ is not directly exposed to any chemicals or polymers before encapsulation to enable a pristine channel free from process-induced damages and polymer residues. However, the purpose of the hBN on our device is to facilitate area-selective contact doping and to show that the device characteristics can be drastically enhanced with contact resistance improvement without adopting measures to improve the channel. The fabrication recipe is similar to blanked exposure devices with an added step of dry-transferring a patterned hBN flake using a
Figure 4.11: Improved device characteristics by selective-area doping of the contact. (a) Optical microscope image for the 3L WSe$_2$ device with a patterned hBN on the channel before UV-O$_3$ exposure. (b) Schematic of the device after oxidation with 2L WSe$_2$ + 1L TOS at the contacts and 3L WSe$_2$ in the channel region. (c) Transfer characteristics before and after contact doping showing 4 order of improvement in the p-type on current. (d) Total contact resistance ($2R_C$) + doped source-drain extension resistance ($2R_{ext}$) and channel resistance ($R_{CH}$) of the device after (red) doping. $L_{CH}$ and $2L_{ext}$ are the length of channel underneath the hBN and the total length of the doped source-drain extension near contact 1 and 2. Poor quality of contacts before oxidation precludes us from extracting these values in the undoped device. (e) Output characteristics of the device before (left) and after (right) contact-doping at room temperature. The effective channel length, $L_{CH}$ reduces from 19 μm (left) to 10 μm (right) after exposure. However, no change in expected in the hBN covered channel after doping. Linear current-voltage characteristics for all applied $V_{DS}$ values (right) proves the ohmic nature of the contacts after oxidation.
polycaprolactone (PCL) polymer stamp onto the etched WSe$_2$. The polymer was then washed off with acetone and Pd/Au (20/50 nm) electrodes were fabricated with e-beam lithography followed by metal deposition. No special treatment such as annealing was performed for an ultraclean surface before $h$BN transfer or metal deposition. Electrical characterization of this device was performed in a probe-station at a vacuum of 10$^{-5}$ mbar before and after oxidation. Post-oxidation schematic of the device is shown in fig. 4.11b. The transfer characteristics of the device as seen in Figure 4.11c appear poor in comparison to our previous devices without $h$BN, possibly due to polymer residue beneath the metal contacts left from the stamp used during the transfer process [100]. Post-oxidation, the uncovered regions of the device near the contacts are converted to 2L WSe$_2$ + 1L TOS as shown in the schematic in Figure 4.11b and we observe 4 orders of enhancement in the p-type current and a positive shift in the threshold voltage in Figure 4.11c. In the contact-doped device, we calculate $R_{CH}$ at $V_{GS} = -100$ V as $\sim 1 \, M\Omega \, \mu m$ from 4-probe measurements, whereas the total resistance of the doped source-drain region ($2R_{ext}$) and metal-semiconductor contacts ($2R_C$) as $32 \, k\Omega \, \mu m$. To decouple $2R_C$ and $2R_{ext}$, we approximate the range for $2R_{ext}$ for the doped region (length $2L_{ext} = 9 \mu m$, width $W = 1 \mu m$) as 30.6–31.5 kΩ·μm using $2R_{ext} = R_S \times 2L_{ext}/W$ where $R_S$ is the sheet resistance values estimated from the devices without $h$BN (3.4–3.5 kΩ·μm). With this calculated range of $2R_{ext}$, we estimate $2R_C$ as 0.75–1.4 kΩ·μm at $V_{GS} = -100$ V. It should be noted that this low $2R_C$ value for area-selective doping lies in the similar range as extracted from the blanket exposure devices, however, we attain a current on-off ratio of 6 orders with contact doping not present in the latter case. This is indicative of better gate-controlled electrostatics achieved through selectively exposing only the contact region to oxidation. Further, the mobility of the channel covered with $h$BN was calculated as 167 cm$^2$/V·s, almost 3 times higher than what we found in blanket exposure channels.
Moreover, as length scaling of resistance applies to the highly doped region, $2R_{\text{ext}}$ can be minimized by reducing the length of the exposed area to have values smaller than $2R_C$ begetting the possibility of high-current devices with careful design consideration. Finally, the non-linear output characteristics with small values of current as seen on the left in Figure 4.11e shows the poor quality of highly resistive Schottky contacts before UV-O$_3$ treatment. Without any measures to enhance the channel covered with hBN, we observe a complete shift towards linear current-voltage relationship for the entire range of applied $V_{DS}$ ($-1\ V$ to $1\ V$) post-oxidation shown on the right in Figure 4.11e, establishing the ohmic nature of the contacts and 4 orders of magnitude improvement in the p-type current just by contact engineering.

4.4 Chapter summary

In conclusion, we demonstrated an area selective doping method for WSe$_2$ using a single layer of dopant, TOS. This nonstoichiometric oxide formed by oxidation of WSe$_2$ with O$_3$ and UV light induces one of the highest hole densities reported so far for WSe$_2$ and enables a route to fabricate low-resistance ohmic contacts to ultra-thin WSe$_2$. Using this method, we show the lowest p-type contact resistance to WSe$_2$ of less than 5 nm thickness. In future work, the performance of the hBN covered field-effect transistor can further be improved by devising ways to fabricate short-length doped regions and to make cleaner metal-semiconductor interfaces during metalization, thereby gaining higher on-current from the channel and employing our doping method to achieve the best contacts. This process of doping is chemical-free and does not require any high-temperature processing or activation, thereby promising a way to fabricate high-performance p-type devices with WSe$_2$ for both room-temperature and low-temperature applications.
Chapter 5

Conclusions and Future Work

Over the course of this thesis, we studied two of the major theoretical and experimental challenges in 2D semiconductor device research and worked out the respective solutions. Considering the vastness of the field, the problems and the solutions we discussed constitute just a tiny portion of everything there is to study for the real-world implementation of these devices. Despite how far we still need to go before we can make reliable 2D vdW devices for electronics, our efficient method to understand their electrostatics and the demonstration of the lowest p-type ohmic contacts to one of the most widely studied 2D semiconductor make a significant contribution towards advancing the field and opens an avenue for novel device designs and intriguing experiments.

5.1 Summary of the theory work

First, we provided insight into the complexities of 2D devices that appear simple and the challenges in simulating and understanding the channel potential and charge distribution on the layers of an arbitrary stacked 2D device. To address these challenges, we derived an equivalent circuit model for the vertical electrostatics of a vdW heterostruc-
ture from the out-of-plane energy band diagram that provides an intuitive explanation of the circuit elements. Our model consists of basic elements such as capacitors and voltage sources and can be easily solved by applying KVL. We also provide a modified definition for the quantum capacitance of the 2D layers that efficiently captures the change in the difference between the conduction band and Fermi level upon application of voltages resulting in the change in charge. We included the work function difference among the materials in the heterostructure as fixed voltage sources. The thickness of 2D materials, if needed to be considered, can be accounted for by adding the associated thickness-dependent geometric capacitance to the geometric capacitance of the adjacent dielectric layer. Our technique is capable of handling non-idealities such as trap states by considering them as capacitive elements. Further, we show that by using Fermi-Dirac statistics instead of Maxwell-Boltzmann approximation, our model is capable of handling both non-degenerate and degenerate carrier concentrations. Although the direct solution of the equivalent circuit for an $n$-layer structure is not possible due to the variable, non-linear quantum capacitance of each layer, an efficient method for solving the circuit is provided using a physics-based approach using Gauss’ law and charge-neutrality condition under quasi-equilibrium. Our method enabled simulation of the potential landscape and charge distribution of an arbitrary number of layers of 2-D semiconductors, graphene, or metals with different work functions stacked into a vdW structure and with different applied voltages. We further, developed an open-source tool, 2dmatstack, on nanohub.org for the nanoscale device community to simulate the vertical electrostatics of novel vdW structures and demonstrated how this tool can be used to predict the behavior of devices such as graphene-based hot-electron transistor with different applied voltages to different layers.
5.2 Future directions for the theory work

The model that we presented can be further developed into a compact model to capture the out-of-equilibrium transport and dynamic characteristics of vdW devices. The following are the proposed improvements to the model–

(i) Incorporate separate quasi-Fermi levels for electrons and holes to account for out-of-equilibrium transport;

(ii) Find the potential at equally spaced lateral grid points in the layers by solving the equations for the vertical cross-sections through those points;

(iii) Solve the semi-classical drift equation from the potential at those points;

(iv) Include second-order non-ideal effects such as mobility degradation and self-heating;

and

(v) Incorporate Schrodinger equation to capture quantum-mechanical and tunneling effects.

5.3 Summary of the experimental work

In the experimental section of this thesis, we resolved the bottleneck of large p-type contact resistance to ultrathin WSe\textsubscript{2}. Despite the vast research on 2D semiconductor devices and methods to fabricate reliable n-type contacts to ultrathin MoS\textsubscript{2}, robust low-resistance ohmic contacts to ultrathin WSe\textsubscript{2} had not been demonstrated before this work. We found that all of the results with contact resistance below 1 k\textOmega \textmu m were demonstrated for thick multilayer samples. To form truly 2D FETs and heterojunctions showing superior performance to Si-based devices, it was crucial to find a way to form low resistance
p-type ohmic contacts to WSe$_2$. To achieve this goal, we developed and optimized an oxidation technique using UV-O$_3$ that forms an oxide, TOS, which dopes the WSe$_2$ layers underneath p-type with carrier densities as high as $4 \times 10^{13}$ cm$^{-2}$. Such a high carrier density results in lowering the sheet resistance of the semiconductor and results in a thinner Schottky barrier at the contact edge. These thin barriers facilitate higher tunnel currents resulting in high-performance ohmic contacts. We optimize the oxidation process for monolayer precision and showed that the TOS formed was only a monolayer thick with optical and AFM characterization. Sub-stoichiometry and amorphous nature of TOS was confirmed by EDS and TEM studies.

With fabrication and 4-probe electrical characterization of multiple ultrathin devices (3L or $\sim$2 nm thick), we demonstrated a consistently reliable method to achieve doping densities in the range 3–4$\times$10$^{13}$ cm$^{-2}$. This results in the lowest reported value of contact resistance for below 5 nm thickness WSe$_2$ so far as 0.6 k$\Omega$.\mu$m. Moreover, in all of our devices we have shown a 300$\times$ improvement in contact resistance value and transition of non-linear output characteristics to linear for all applied source-drain bias ranges which are indicative of the fact that the initial poor performance of the as-fabricated devices was insignificant after doping. We also performed temperature-dependent electrical characterization to show that these contacts retain their ohmic nature at temperatures as low as 77 K. Further electrical characterization taken 4 months apart on devices kept in the ambient without any encapsulation showed minimal degradation in performance demonstrating the stability of our doping.

Next, we show the area selectivity of our contact doping on a device where a layer of hBN was transferred to cover the channel region after fabrication. Without any special treatment to enhance the channel properties, this device showed 4 orders of on-current improvement with more than 6 orders of on-off ratio for p-type transport and a complete
shift from non-linear Schottky behavior to linear output characteristics after doping.

5.4 Future direction for the experimental work

Solving the contact resistance issue to WSe$_2$ opens the door to novel devices and experiments. A roadmap for some of the near-future projects is presented below.

5.4.1 Mechanism of doping

The proposed hypothesis for how substoichiometric oxides dope the material underneath is called substrate charge transfer doping (SCTD) mechanism. This is a known mechanism for many other material systems such as diamond [101], organic semiconductors [102] and III-IV [103] semiconductors using a different dopant species and relies on charge separation at the interface. The dopant species is expected to place a concentration of charges or dipoles at the interface which dopes the material underneath with opposite polarity. Although widely studied for other material systems, TOS requires further structural, optical, and electrical characterization to confirm that it indeed works via SCTD mechanism.

5.4.2 Further improvement in contact resistance

In our scheme of fabrication, we perform UV-O$_3$ treatment of the device after metalization to avoid any further processing of the TOS layer. Therefore, the area directly beneath the metal is likely to not get oxidized. However, in studies performed by Arutchel-van et al. on a metal-MoS$_2$ interface, it was found that for thin films doping the edge of the contact is more effective than doping the complete region under the contact [72]. Although it is reasonable to assume that majority of the current is injected at the heavily doped, low-resistance edge and the area directly beneath the metal contacts do not play
a significant role in the injection, a detailed experimental investigation remains open for future studies. With a fabrication scheme that dopes both the regions underneath and at the edge of the metal, it could be possible to lower the contact resistance further in these devices.

5.4.3 Demonstration of near ideal 2D devices

Although in this work we showed the best p-tye contact results for WSe$_2$ and area selectivity of the doping, we did not focus on fabrication of a near-ideal 2D pFET or high-performance TFETs. With modification and optimization in the recipe, it possible to fabricate ultraclean WSe$_2$ device encapsulated between hBN with dual gate structure, thinner gate dielectric, and doped contacts. While the doped contacts enable high current injection, pristine quality of the channel (free from damages and polymer residues) and excellent gate electrostatics are expected to result in near-ideal characteristics such as 60 mV/dec sub-threshold slope with no hysteresis. By reducing the channel length to sub-nm scale, its further possible to achieve extremely high current densities. For example, our device with a channel length of 10 $\mu$m and 0.6 k$\Omega$.$\mu$m contact resistance shows 36 k$\Omega$.$\mu$m channel resistance. This implies that given length scaling is applicable, our contacts have the potential to inject 1 mA/um of current into a channel of length 100 nm at 1V V$_{DS}$, as high as standard Si MOSFETs. Moreover, combined with the best contact-engineering methods for MoS$_2$, our method opens the avenue for fabrication and study of superior ultrathin vertical p-n junction and tunnel devices with MoS$_2$-WSe$_2$ heterostructures.

5.4.4 Universality of the method for all 1D, 2D, and 3D materials

Since surface charge transfer mechanism has been demonstrated for multiple material systems, TOS doping is also expected to work on other nanoscale devices such as carbon
Figure 5.1: TOS doping of an organic semiconductor DNTT. (a) Schematic of a 1L-WSe₂ device which was converted to TOS and the DNTT device with the TOS placed below the organic semiconductor. (b) Output characteristics of the device before and after oxidation. (c) Transfer characteristics of the device before and after oxidation showing strong hole doping and 4 orders of improvement in p-type on-current.

nanotube (CNT), organic semiconductors, graphene, all other 2D semiconductors, and III-IV systems. As proof of concept, we demonstrated the initial results on an organic semiconductor–DNTT. We fabricated two devices with DNTT, a typical p-type organic semiconductor — one device included a layer of TOS on the bottom of the channel while the other did not, as shown in fig. 5.1(a). To begin with, we exfoliated 1L-WSe₂ on a SiO₂/Si substrate followed by lift-off metallization with Ti/Pd/Au (2/20/20 nm). 1L-WSe₂ was converted into monolayer TOS through UV-O₃ oxidation. Contacts were also concurrently patterned in areas without TOS to form the second device. Then, 40 nm of DNTT was deposited by sublimation. The channel areas were defined by coating the sample with PMMA, patterning with e-beam lithography, and etching away the semicon-
ductor with SF$_6$ plasma, leaving the active channel area (see fig. 5.1(a)). As shown in fig. 5.1(b) and (c), the transistor characteristics are significantly improved in the device with the TOS layer resulting in a much improved on/off ratio, reduced threshold voltage, and higher p-branch current compared to the device without the TOS-layer. However, the TOS-doped DNTT device shows transistor-like characteristics in contrast to the resistor-like characteristics seen from TOS-doped WSe$_2$. This could be attributed to the much larger thickness of DNTT (~40 nm) and the placement of TOS on the bottom of the channel. Overall, the electrical characterizations show that TOS can provide universal p-type doping to a wide range of semiconducting materials that results in improved device characteristics.
References


C. M. Smyth, R. Addou, S. McDonnell, C. L. Hinkle, and R. M. Wallace, “Wse\textsubscript{2} -contact metal interface chemistry and band alignment under high vacuum and


Appendix A

The following code was written in MATLAB and input/output (I/O) sections have been modified according to the I/O interface of nanohub.org. While simulating on MATLAB, these commands are required to be modified according to the environment. Temperature can be modified in the constants section. Functions f_graphene and f_semi calculate the carrier densities using Fermi-Dirac statistics in graphene and 2D semiconductors respectively. Polylog_octave function is written to compute the Fermi-Dirac integration more efficiently.
%% Material 1 | Dielectric 1 | Material 2 | Dielectric 2 | Material 3 ....
%% Program Flow: Input.m->Fermi_Dirac_distributions.m->main_program.m->
% Energy_Band_Diagrams.m

%% ========= Constants and value assignment ============
constants; % Calls the program having constants such as electron
% charge, boltzman constant etc.
mixal=1; semiconductor=2; graphene=3;
io = rpLib(infile);

%% ==============Input parameters ===============
% Material specification
number_of_plates = int32(rpLibGetDouble(io,['input.integer' ...
    '(number_of_plates).current'])); %User input
number_of_plates;
material = []; %User input, The array "material" should have
% same number points as number_of_plates
for i=1:number_of_plates
    material = [material rpLibGetDouble(io,['input.group(Material_' ...
        num2str(i) ').choice(material).current'])];
end

% Band Gap for 2D semiconductor, or metal and graphene by default 0
% Band Gap for 2D semiconductor, or metal and graphene by default 0
bandgap = []; %User input
for i=1:number_of_plates
    bandgap = [bandgap rpLibGetDouble(io,['input.group(Material_' ...
        num2str(i) ').number(bandgap).current'])];
    if (material(i) ~= semiconductor)
        bandgap(i) =0;
    end
end

% Acceptor and donor concentration for 2D semiconductor and graphene
N_A = []; %User input
N_D = []; %User input
for i=1:number_of_plates
    N_A = [N_A rpLibGetDouble(io,['input.group(Material_' ...
        num2str(i) ').number(N_A).current'])];
    N_D = [N_D rpLibGetDouble(io,['input.group(Material_' ...
        num2str(i) ').number(N_D).current'])];
end

% Electron affinities and work functions
electron_affinity = []; %User input
work_function = []; %User input
for i=1:number_of_plates
    if material(i) ~= metal
        electron_affinity = [electron_affinity rpLibGetDouble
            (io,['input.group(Material_' ...
            num2str(i) ').number(electron_affinity).current'])];
    elseif material(i) == metal
        % Code for metal
    end
end
electron_affinity = [electron_affinity rpLibGetDouble
    (io,['input.group(Material_' num2str(i) ').number(work_function).current'])];
end

%Applied voltages
V=[];              %User input
for i=1:number_of_plates
    V = [V rpLibGetDouble(io,['input.group(Material_' ... 
        num2str(i) ').number(V).current'])];
end

% If semiconductor, ask for effective mass for each, N/A for metal
effective_mass_electron = []; %User input
for i=1:number_of_plates
    effective_mass_electron = [effective_mass_electron 
        rpLibGetDouble(io,['input.group(Material_' ... 
        num2str(i) ').number(effective_mass_electron).current'])];
end

effective_mass_hole = []; %User input
for i=1:number_of_plates
    effective_mass_hole = [effective_mass_hole rpLibGetDouble(io, ... 
        ['input.group(Material_' ... 
        num2str(i) ').number(effective_mass_hole).current'])];
end

%For each dielectric have to specify the thickness, electron affinity and bandgap
Thickness_dielectric = [];
Dielectric_constant = [];
Electron_affinity_dielectric = [];
Bandgap_dielectric = [];
for i=1:number_of_plates-1
    Thickness_dielectric = [Thickness_dielectric rpLibGetDouble(io, ... 
        ['input.group(Dielectric_' ... 
        num2str(i) ').number(Thickness_dielectric).current'])];
    %User input
    Dielectric_constant = [Dielectric_constant ... 
        rpLibGetDouble(io,['input.group(Dielectric_' ... 
        num2str(i) ').number(Dielectric_constant).current'])]; %User input
    Electron_affinity_dielectric(i) = 0;                  %User input
    Bandgap_dielectric(i)= 7;                  %User input
end

% ========= Parameters required only for plotting EBD ==============
Vacuum_level=0;

%define spatial positions for band diagram, 2 points for each plate
EBD_Thickness = zeros(1,2*number_of_plates-1);
for i=1:number_of_plates
    EBD_Thickness(2*i-1)= 1;
end
for i=1:number_of_plates-1
    EBD_Thickness(2*i) = Thickness_dielectric(i);
EBD_Thickness = EBD_Thickness .* 1e-7;

%% === Material specifications that need to be calculated by the program ======
mass_Semiconductor_CB = effective_mass_electron*m_o;
mass_Semiconductor_VB = effective_mass_hole*m_o;
DOS_CB_Semiconductor = mass_Semiconductor_CB/(pi*hbar^2);
DOS_VB_Semiconductor = mass_Semiconductor_VB/(pi*hbar^2);

% CB density of states of each plate
DOS_CB = zeros(1,number_of_plates);
for i=1:number_of_plates
    if material(i) == 2
        DOS_CB(i) = DOS_CB_Semiconductor(i);
    end
end

% VB density of states of each plate
DOS_VB = zeros(1,number_of_plates);
for i=1:number_of_plates
    if material(i) == 2
        DOS_VB(i) = DOS_VB_Semiconductor(i);
    end
end

%Initial difference between Fermi level and the conduction band edge
Ec_Ef_initial = [];   %calculated here
range= [-10 10];  %Range to search for Ec-Ef_initial
for i=1:number_of_plates
    if (material(i) == semiconductor)
        fun_semi = @(x)f_semi(x,i,N_A, N_D, DOS_CB, DOS_VB, bandgap);
        %defined a function to calculate Ec-Ef_initial from donor and acceptor concentrations in semiconductor
        x = fzero(fun_semi,range);
        Ec_Ef_initial(i) = x;
    elseif (material(i) == graphene)
        fun_graphene = @(x)f_graphene(x,i,N_A, N_D);  %defined a function
        % to calculate Ec-Ef_initial from donor and acceptor concentrations in graphene
        x = fzero(fun_graphene,range);
        Ec_Ef_initial(i) = x;
    elseif (material(i) == metal)
        Ec_Ef_initial(i) =0;
    end
end

Capacitance_dielectric = Dielectric_constant.*eps_o./ (Thickness_dielectric.* 1e-7);
%% ==========Call function for Fermi-Dirac distributions============
[fQ_TMDC,fQ_graphene] = Fermi_Dirac_distribution(bandgap, Ec_Ef_initial,DOS_CB, DOS_VB);

%% ======================Call Main Program ============================
% First, if there are metal plates in between the first and last material
% in the stack we divide the entire stack into substacks whenever we
% encounter a metal as- meta| 2D semiconductor or graphene|...metal
index_interior_metals=[];
j=1;
for i=2:number_of_plates-1 % find interior metal plates
    if material(i) == metal
        index_interior_metals(j) = i;
        j=j+1;
    end
end
Q = zeros(1,number_of_plates);
Ec_Ef = zeros(1,number_of_plates);
phi_ox= zeros(1,number_of_plates-1);
N= zeros(1,number_of_plates);

% Then we solve each sub-stack separately and add the calculated
% solution arrays for each stack at the end of the solution for
% last stack to find the complete solution
for j = 1:1+length(index_interior_metals)
    % set start_index
    if j==1
        start_index = 1;
    else
        start_index = index_interior_metals(j-1);
        % this is the last used end_index
    end
    % set end_index
    if j > length(index_interior_metals)
        end_index = number_of_plates;
    else
        end_index = index_interior_metals(j);
    end
    [Q_sub, Ec_Ef_sub, phi_ox_sub, N_sub] = main_program(start_index,end_index,fQ_TMDC, fQ_graphene,...
V, material,Ec_Ef_initial, electron_affinity,Capacitance_dielectric);
% add solution values for sub problem to the global solution
Q(1,start_index:end_index) = Q(1,start_index:end_index) + Q_sub;
Ec_Ef(1,start_index:end_index) = Ec_Ef(1,start_index:end_index) + Ec_Ef_sub;
phi_ox(1,start_index:end_index-1) = phi_ox(1,start_index:end_index-1) + phi_ox_sub;
N(1,start_index:end_index) = N(1,start_index:end_index) + N_sub;
end

tab = char(9);
extline = char(10);
data0 = []; for i=1:number_of_plates
  data0 = [data0 ' Layer ' num2str(i)]; end

data1 = ['Q_net:', num2str(Q, ' %10.3e 	'), newline];
data2 = ['p-n:', num2str(N, ' %10.3e 	'), newline];
data3 = ['Ec-Ef:', num2str(Ec_Ef, ' %10.3e	'), newline];
data4 = ['\phi:', num2str(phi_ox, ' %10.3e\t')];
data = [line1, line2, line3, line4, data0, data1, data2, data3, data4];

%% ============= Call Energy Band Diagram Plotting ===================
[pos, Ec_bc, Ev_bc, Ef_bc, Ec_biais, Ev_biais, Ef_biais, pos_discrete,
  Ec_bc_discrete, Ef_bc_discrete, Ev_bc_discrete] =
  Energy_Band_Diagrams (Ec_Ef, EBD_Thickness, Vacuum_level, ...
  electron_affinity, Ec_Ef_initial, Electron_affinity_dielectric,...
  Bandgap_dielectric, bandgap, V, number_of_plates, phi_ox); 
pos = pos *1e7; 
xydata = [pos;Ef_bc]; 
rlPutString(io,'output.curve(Ef_bc).component.xy',str,0); 
xydata = [pos;Ec_bc]; 
rlPutString(io,'output.curve(Ec_bc).component.xy',str,0); 
xydata = [pos;Ev_bc]; 
rlPutString(io,'output.curve(Ev_bc).component.xy',str,0);

for i=1:number_of_plates
  xydata = [pos_discrete(i,:), Ef_bc_discrete(i,:)]; 
end
str = sprintf('%12g %12g\n', xydata); 
rlPutString(io,'output.curve(Ef_bc_discrete).component.xy',str,1); 

for i=1:number_of_plates
  xydata = [pos_discrete(i,:), Ec_bc_discrete(i,:)];
end
str = sprintf('%12g %12g
', xydata);
rpLibPutString(io,'output.curve(Ec_bc_discrete).component.xy',str,1);

for i=1:number_of_plates
    xydata = [pos_discrete(i,:), Ev_bc_discrete(i,:)];
    str = sprintf('%12g %12g
', xydata);
    rpLibPutString(io,'output.curve(Ev_bc_discrete).component.xy',str,1);
end

xydata = [pos;Ef_bias] ;
str = sprintf('%12g %12g
', xydata);
rpLibPutString(io,'output.curve(Ef_bias).component.xy',str,0);

xydata = [pos;Ec_bias] ;
str = sprintf('%12g %12g
', xydata);
rpLibPutString(io,'output.curve(Ec_bias).component.xy',str,0);

xydata = [pos;Ev_bias] ;
str = sprintf('%12g %12g
', xydata);
rpLibPutString(io,'output.curve(Ev_bias).component.xy',str,0);

figure;
for i=1:number_of_plates
    if material(i) ~= metal
        plot(pos_discrete(i,:), Ec_bc_discrete(i,:), 'r','linewidth',9);
        hold on; set(gca,'fontsize',26); box on; set(gca,'linewidth',2);
        hold on; ylabel('Energy (eV)'); xlabel('Thickness (nm)');
        xlim([0 2*number_of_plates+1]); ylim([min(Ev_bc) Vacuum_level]);
        plot(pos_discrete(i,:), Ev_bc_discrete(i,:), 'g','linewidth',9);
        hold on; plot(pos_discrete(i,:), Ef_bc_discrete(i,:), '-.b','linewidth',9);
        hold on; legend('Ec', 'Ev', 'Ef');
    elseif material(i) == metal
        plot(pos_discrete(i,:), Ef_bc_discrete(i,:), '-.b','linewidth',9);
        hold on; set(gca,'fontsize',26); box on; set(gca,'linewidth',2);
        hold on; ylabel('Energy (eV)');
        xlim([0 2*number_of_plates+1]); ylim([min(Ev_bc) Vacuum_level]);
    end
    label= ["Layer ", num2str(i)];
    text (2*(i-1)+.2, min(Ev_bc)+1, label);
end
drawnow;
print("isolated_layers.jpeg",'-dpng', '-F:20');
%print -dpng isolated_layers.jpeg;
rpLibPutFile(io,'output.image(snapshot1).current', ...
    'isolated_layers.jpeg',1, 0);
% ===== Fermi-Dirac distribution for each type of material =====
function [fQ_TMDC, fQ_graphene] = Fermi_Dirac_distribution(bandgap, ...
    Ec_Ef_initial, DOS_CB, DOS_VB)

    constants;

    fQ(TMDC) = @(i,Ec_Ef) q*(-DOS_CB(i).*(-kT*(log(exp(-E_f/E_f)+1) - ...
        log(exp(-E_f_initial(i)/kT)+1)))...
        +DOS_VB(i).*(-kT*(log(exp((Ec_Ef-bandgap(i))/kT)+1)...
            - log(exp((Ec_Ef_initial(i)-bandgap(i))/kT)+1))));

    fQ_graphene = @(i,Ec_Ef) q*(2*(kT)^2/(pi*hbar^2*vF^2) * ... 
        (-(-real(Polylog_octave(-exp(-E_f/kT))))...
            -(real(Polylog_octave(-exp(-E_f_initial(i)/kT)))))... 
        +(real(Polylog_octave(-exp(E_f/kT))))...
            +(-real(Polylog_octave(-exp(E_f_initial(i)/kT))))));
function [Q_sub, Ec_Ef_sub, phi_ox_sub, N_sub] = main_program
(start_index,end_index,fQ_TMDC, fQ_graphene,...
V, material,Ec_Ef_initial, ...
electron_affinity,Capacitance_dielectric)

constants;
metal=1; semiconductor=2; graphene=3;
step_Ec_Ef = 1;
set_lb = 1; set_ub = 1;
Ec_Ef_lb = Ec_Ef_initial(1);                   % lower bound in eV
Ec_Ef_ub = Ec_Ef_initial(1);                   % upper bound in eV
tol_exit = 1e-6;
loop = 1;
while loop
    Q_total = 0;
    Q_sub = zeros(1,(end_index-start_index+1));
    Ec_Ef_sub = zeros(1,(end_index-start_index+1));
    phi_ox_sub= zeros(1,(end_index-start_index));
    %%   ===========       metal | metal   ==============
    if material(start_index)==metal && material(start_index+1)==metal
        phi_ox_sub(1)= V(start_index)-V(start_index+1) +
                     electron_affinity(start_index+1)-electron_affinity(start_index);
        Q_sub(1)=Capacitance_dielectric(start_index)* phi_ox_sub(1);
        Q_sub(2)= -Q_sub(1);
        loop=0;
        N_sub=Q_sub/q;
    end
    %%  ===========   metal  | semiconductor or graphene  ===========
    if material(start_index)==metal && material(start_index+1)~=metal
        k=2;
        Ec_Ef_sub(k-1) = 0;
        if set_lb
            Ec_Ef_lb = Ec_Ef_lb - step_Ec_Ef;
            Ec_Ef_guess = Ec_Ef_lb;
        elseif set_ub
            Ec_Ef_ub = Ec_Ef_ub + step_Ec_Ef;
            Ec_Ef_guess = Ec_Ef_ub;
        else
            Ec_Ef_guess = (Ec_Ef_lb + Ec_Ef_ub)/2;
        end
        Ec_Ef_guess = (Ec_Ef_lb + Ec_Ef_ub)/2;
    end
    if material(start_index+1)==semiconductor
        Q_sub(k)= fQ_TMDC(k,Ec_Ef_sub(k));
    elseif material(start_index+1)==graphene
        Q_sub(k)= fQ_graphene(k,Ec_Ef_sub(k));
    end
    Q_total=Q_total+Q_sub(k);
    phi_ox_sub(1)= V(start_index)-V(start_index+1) - Ec_Ef_sub(1)
                 + Ec_Ef_sub(2) + electron_affinity(start_index+1)
                 -electron_affinity(start_index);
    Q_sub(1)= Capacitance_dielectric(start_index)*phi_ox_sub(1);
Q_total=Q_total+Q_sub(1);
for   i=start_index:(end_index-2)
    if k < end_index-start_index+1
        if material(i+2)==metal %metal |
            % semiconductor or graphene| metal
            Ec_Ef_sub(k+1)=0;
            phi_ox_sub(k)=V(i+1)-V(i+2) -
            Ec_Ef_sub(k) + Ec_Ef_sub(k+1)
            + electron_affinity(i+2)-electron_affinity(i+1);
            Q_sub(k+1)= -Capacitance_dielectric(i+1)*phi_ox_sub(k);
            Q_total=Q_total+Q_sub(k+1);
        elseif material(i+2)~=metal           %metal |
            % semiconductor or graphene| semiconductor or graphene |....
            Ec_Ef_sub(k+1) = Q_total/Capacitance_dielectric(i+1)
            - (V(i+1)-electron_affinity(i+1)-Ec_Ef_sub(k))
            + (V(i+2)-electron_affinity(i+2))
            + Ec_Ef_sub(k+1) + electron_affinity(i+2); 
            phi_ox_sub(k)= V(i+1)-V(i+2) - Ec_Ef_sub(k)
            + electron_affinity(i+1);
            if material(i+2)==semiconductor
                Q_sub(k+1)= fQ_TMDC(k+1,Ec_Ef_sub(k+1));
            elseif material(i+2)==graphene
                Q_sub(k+1)= fQ_graphene(k+1,Ec_Ef_sub(k+1));
            end
            Q_total= Q_total+ Q_sub(k+1);
        end
    end
    k=k+1;
end
if set_lb
    if Q_total <= 0
        set_lb = 0;
    end
elseif set_ub
    if Q_total >= 0
        set_ub = 0;
    end
else
    if (abs(Q_total) <= tol_exit*min(abs(Q)))||(Ec_Ef_ub==Ec_Ef_lb)
        loop = 0;
    else
        if Q_total<0
            % need to increase positive charge on first plate
            Ec_Ef_lb = Ec_Ef_guess ;  % brings lower bound up,
            % increasing + charge
        elseif Q_total>0
            Ec_Ef_ub = Ec_Ef_guess ;  % brings upper bound down,
            % increasing - charge
        end
end
end
N_{\text{sub}}=Q_{\text{sub}}/q;
end

%%  =============== semiconductor or graphene =================

if \text{material}(\text{start\_index})== \text{semiconductor} \ ||
\text{material}(\text{start\_index})== \text{graphene}
k=1;

if k < \text{end\_index}-\text{start\_index}+1
    if set_{lb}
        \text{Ec}_{\text{Ef}}_{lb} = \text{Ec}_{\text{ Ef}}_{lb} - \text{step}_{\text{Ec}_{\text{Ef}}};
        \text{Ec}_{\text{Ef}}_{guess} = \text{Ec}_{\text{Ef}}_{lb};
    elseif set_{ub}
        \text{Ec}_{\text{Ef}}_{ub} = \text{Ec}_{\text{ Ef}}_{ub} + \text{step}_{\text{Ec}_{\text{Ef}}};
        \text{Ec}_{\text{Ef}}_{guess} = \text{Ec}_{\text{Ef}}_{ub};
    else
        \text{Ec}_{\text{Ef}}_{guess} = (\text{Ec}_{\text{Ef}}_{lb} + \text{Ec}_{\text{Ef}}_{ub})/2;
    end
    \text{Ec}_{\text{Ef}}_{sub}(k) = \text{Ec}_{\text{Ef}}_{guess};
    if \text{material}(\text{start\_index})==\text{semiconductor}
        Q_{\text{sub}}(k)= f_{\text{Q\_TMDC}}(k,\text{Ec}_{\text{Ef}}_{sub}(k));
    elseif \text{material}(\text{start\_index})==\text{graphene}
        Q_{\text{sub}}(k)= f_{\text{Q\_graphene}}(k,\text{Ec}_{\text{Ef}}_{sub}(k));
    end
end
\text{Q\_total}=\text{Q\_total}+Q_{\text{sub}}(k);
for \text{i}=\text{start\_index}:\text{end\_index}-1
    if \text{material}(\text{i+1})==\text{metal} \ % \text{semiconductor} \ | \ \text{metal}
        \text{Ec}_{\text{Ef}}_{sub}(k+1)=0;
        \text{phi}_{\text{ox}}_{sub}(k)=V(i)-V(i+1) - \text{Ec}_{\text{Ef}}_{sub}(k) + \text{Ec}_{\text{Ef}}_{sub}(k+1)
        + \text{electron\_affinity}(i+1)-\text{electron\_affinity}(i);
        Q_{\text{sub}}(k+1)= -\text{Capacitance\_dielectric}(i)\times\text{phi}_{\text{ox}}_{sub}(k);
        \text{Q\_total}=\text{Q\_total}+Q_{\text{sub}}(k+1);
    elseif \text{material}(\text{i+1})==\text{metal} \ % \text{semiconductor} \ | \ \text{semiconductor} \ | \ ....
        \text{Ec}_{\text{Ef}}_{sub}(k+1) = \text{Q\_total}/\text{Capacitance\_dielectric}(i)
        - (V(i)-\text{electron\_affinity}(i)-\text{Ec}_{\text{Ef}}_{sub}(k))
        + (V(i+1)-\text{electron\_affinity}(i+1));
        \text{phi}_{\text{ox}}_{sub}(k)=V(i)-V(i+1) - \text{Ec}_{\text{Ef}}_{sub}(k)
        + \text{Ec}_{\text{Ef}}_{sub}(k+1) + \text{electron\_affinity}(i+1)-\text{electron\_affinity}(i);
        if \text{material}(\text{i+1})==\text{semiconductor}
            Q_{\text{sub}}(k+1)= f_{\text{Q\_TMDC}}(k+1,\text{Ec}_{\text{Ef}}_{sub}(k+1));
        elseif \text{material}(\text{i+1})==\text{graphene}
            Q_{\text{sub}}(k+1)= f_{\text{Q\_graphene}}(k+1,\text{Ec}_{\text{Ef}}_{sub}(k+1));
        end
        \text{Q\_total}=\text{Q\_total}+Q_{\text{sub}}(k+1);
    end
    k=k+1;
end

% k=k+1;
if set_{lb}
    if \text{Q\_total} \leq 0
        set_{lb} = 0;
    end
elseif set_ub
if Q_total >= 0
set_ub = 0;
end
else
% if (abs(Q_total) <= tol_exit*min(abs(Q))) ||
% Ec_Ef_lb==Ec_Ef_ub
% % || (abs(Q_total) < Q_exit)
if (abs(Q_total) <= tol_exit*min(abs(Q_sub)))
% ||(abs(Ec_Ef_ub-Ec_Ef_lb)<=1e-20)
loop = 0;
else
if Q_total<0          % if Q < 0, need to increase positive
% charge on first plate
Ec_Ef_lb = Ec_Ef_guess ;    % brings lower bound up,
% increasing + charge
elseif Q_total>0
Ec_Ef_ub = Ec_Ef_guess   ;  % brings upper bound down,
% increasing - charge
end
end
end
end
N_sub=Q_sub/q;
end
end
function [pos, Ec_bc, Ev_bc, Ef_bc, Ec_bias, Ev_bias, Ef_bias, pos_discrete, ...  
    Ec_bc_discrete, Ef_bc_discrete, Ev_bc_discrete] = Energy_Band_Diagrams ...  
    (Ec_Ef, EBD_Thickness, Vacuum_level, electron_affinity, Ec_Ef_initial, ...  
    Electron_affinity_dielectric, Bandgap_dielectric, bandgap, V, number_of_plates, phi_ox)

delta = 1e-11; % separation between two consecutive points on adjacent materials
pos = zeros(1, 2*length(EBD_Thickness)); % Each material is defined by two points
for i = 1:length(EBD_Thickness)
    if (i==1)
        pos(2*i-1) = 0;
        pos(2*i) = pos(2*i-1) + EBD_Thickness(i);
    else
        pos(2*i-1) = pos(2*i-2) + delta;
        pos(2*i) = pos(2*i-1) + EBD_Thickness(i);
    end
end

% CONTINUOUS, USED FOR JUST CALCULATION IN POST-BIAS
Ec_bc = zeros(1, length(pos));
Ef_bc = zeros(1, length(pos));
E_gap = zeros(1, length(pos));
for i = 1:1:1
    Ec_bc(4*i-3) = Vacuum_level - electron_affinity(i);
    Ec_bc(4*i-2) = Vacuum_level - electron_affinity(i);
    Ef_bc(4*i-3) = Ec_bc(4*i-3) - Ec_Ef_initial(i);
    Ef_bc(4*i-2) = Ec_bc(4*i-2) - Ec_Ef_initial(i);
    E_gap(4*i-3) = bandgap(i);
    E_gap(4*i-2) = bandgap(i);
end
for i = 1:(number_of_plates-1)
    Ec_bc(4*i-1) = Vacuum_level - Electron_affinity_dielectric(i);
    Ec_bc(4*i) = Vacuum_level - Electron_affinity_dielectric(i);
    Ef_bc(4*i-1) = Ec_bc(4*i-1) - Bandgap_dielectric(i)/2;
    Ef_bc(4*i) = Ec_bc(4*i) - Bandgap_dielectric(i)/2;
    E_gap(4*i-1) = Bandgap_dielectric(i);
    E_gap(4*i) = Bandgap_dielectric(i);
end

for i = 1:(number_of_plates-1)
    delta_Ecf(2*i-1) = Ec_bc(4*i-1) - Ec_bc(4*i-2);
    delta_Ecf(2*i) = Ec_bc(4*i) - Ec_bc(4*i+1);
end

% conduction band edge differences

Ev_bc = Ec_bc - E_gap;
delta_Ecf = zeros(1, 2*(number_of_plates-1));
for i = 1:1:1
    delta_Ecf(2*i-1) = Ec_bc(4*i-1) - Ec_bc(4*i-2);
    delta_Ecf(2*i) = Ec_bc(4*i) - Ec_bc(4*i+1);
end

% Ec, Ef and Ev, before contact (abbr. _bc)
% Constants
% thermal energy in eV (at 300 K)
kT = 0.0259;

% in eV/K, Boltzmann constant
k = 8.617e-5;

vF = 1e8;
T = 300;
kT = k*T;

% eV*s
hbar = 6.58e-16;

% cm/s
c = 3e10;

% MeV/c^2 = [eV*s^2/cm^2]
m_o = 0.511e6/(c^2);

% C
q = 1.602e-19;

% F/cm (8.85e-12 F/m)
eps_o = 8.85e-14;
```matlab
function y = f_graphene(x, i, N_A, N_D)
    constants;
    y = q*(N_D(i) - N_A(i) + 2*(kT)^2/(pi*hbar^2*vF^2)*...
            (-real(Polylog_octave(-exp(-x/kT)))...
            + real(Polylog_octave(-exp(x/kT)))));
```
function y = f_semi(x,i,N_A, N_D, DOS_CB, DOS_VB, bandgap)
constants;
y = q*(N_D(i) - N_A(i)  +  kT*(DOS_CB(i)*(-log(exp(-x/kT)+1))...
+DOS_VB(i)*log(exp((x-bandgap(i))/kT)+1)));

function [polylog_value]= Polylog_octave(argument)
polylog_sum=0;
if abs(argument)<1
    for n=1:40
        sum=argument^n./n^2;
polylog_sum= sum+polylog_sum;
    end
polylog_value=polylog_sum;
else for n=1:40
    sum=(1/argument)^n./n^2;
polylog_sum= sum+polylog_sum;
end
polylog_value=-polylog_sum - pi^2/6 - .5*(log(-argument))^2;
end
end