Heterogeneous Integration in Switchmode Electronics

Kevin Tien

Submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Graduate School of Arts and Sciences

Columbia University

2019
ABSTRACT

Heterogeneous Integration in Switchmode Power Electronics

Kevin Tien

This dissertation looks closely at deployment of thin-film integrated inductors within power electronics, including details on the state-of-the-art technology for such inductors and related packaging techniques. Design challenges for systems using these inductors are discussed in detail, including the current outlook on magnetics development and the impact of these non-linearities on system design. In particular, this work looks closely at effects often left behind in modern discrete-component-based power module design, such as soft core saturation and significant high-frequency losses.

In conjunction with the magnetics, a well-known non-linear controller for buck converters is analyzed in-depth for the first time, using frameworks from variable structure and sliding-mode control. This allows for development of a more profound rationale for the heuristic design guidelines that have been heretofore provided for this class of controllers.

To verify the theoretical development, a testbench integrated CMOS front-end for a switched-inductor step-down, or buck converter is used to investigate departures of system behavior from the general wisdom around buck converter performance. Two packaging methodologies are explored for integration, and their impact on the design cycle and module lifetimes are discussed in some detail.
Contents

List of Figures iii

List of Tables vi

Acknowledgements vii

Introduction 1

1 CMOS-Compatible Power Inductors 4

1.1 Switched-Inductor Converters 5

1.2 Power Inductors 20

2 Control of Buck Converters 45

2.1 Formulating LTI Approximate Systems 46

2.2 LTI Control Design 49

2.3 Variable-Structure Systems 54

2.4 The Bang-Bang Buck Control Family 56

2.5 Asymptotic Stability of One Class of Bang-Bang Controller 59

2.6 Injection Locking for Fixed Switching Frequency Behavior 63

3 Packaging and Testing of Switched-Thin-Film-Inductor Buck Converters 70
List of Figures

1.1 The ideal boost converter ......................................................... 6
1.2 The ideal buck converter ......................................................... 11
1.3 The ideal buck converter cast as an LTI system with time-varying input ......................................................... 12
1.4 ................................................................................................. 14
1.5 Soft-switching/quasi-resonant converter examples ......................................................... 15
1.6 Material descriptive curves for Permalloy ......................................................... 26
1.7 Buck converter steady-state inductor current waveform in a soft-saturating inductor ......................................................... 29
1.8 A spiral inductor implemented in a CMOS back end, from [41] ......................................................... 30
1.9 A yoke inductor implemented in a CMOS-compatible process, from [46] ......................................................... 31
1.10 A stack-up for a solenoidal inductor in a CMOS back end, from [52] ......................................................... 32
1.11 Measured small-signal AC resistance plot for a yoke-construction device, courtesy of Phil Herget ......................................................... 37
1.12 One period of an asymmetric triangle wave ......................................................... 39
1.13 THD vs. duty cycle for an ideal buck converter ......................................................... 40
1.14 Fundamental amplitude assuming constant peak-to-peak ripple and peak-to-peak inductor current ......................................................... 43
THD and fundamental component magnitude in simulated buck converter run at 50% duty cycle, deploying a soft-saturating inductor

An example of voltage-mode control

An example of current-mode control

Circuits for the bang-bang controller

A target switching trajectory with an unstable neighborhood

A potential, undesired trajectory if a varying switching surface alone is used, from [5]

An injection-locking augmentation to the bang-bang controller

Schematic of converter circuitry, from [59]

Layout image of IO pattern for silicon die

Representative M-H curves for the magnetic material used on the interposer. The red curve is the hard axis, and the blue curve the easy axis.

The Finetech FINEPLACER lambda

Illustration of the interposer-based module stack

Illustration of the IPD-based module stack

Sequential close-ups of the interposer module stack-up, originals courtesy of Jae-woong Nah

Interposer layout, courtesy of Naigang Wang

Efficiency vs. load current at varying \(V_{in}\), interposer module

Efficiency vs. input voltage with fixed load current, interposer module

Transient start-up of interposer based system
3.14 Output voltage vs. duty cycle for IPD-based system; four phase at per-phase switch-ing frequency of 100 MHz, input of 1.8 V . . . . . . . . . . . . . . . . . . . . . . . . . . . 85

3.15 Efficiency vs. duty cycle, IPD-based module . . . . . . . . . . . . . . . . . . . . . . . . 86

3.16 Efficiency vs. duty cycle, simulated with Ferric Inc. physics-based thin-film inductor model, 15 MHz switching frequency . . . . . . . . . . . . . . . . . . . . . . . . 87

3.17 Efficiency vs. frequency, IPD-based module . . . . . . . . . . . . . . . . . . . . . . . . 87
List of Tables

1.1 Comparison of integrated inductors .............................................. 33

3.1 Inductor technology summary ..................................................... 74
Acknowledgements

Much of the effort spent during my graduate travels (travails?) is not actually reflected herein, for my sins. The design cycles for circuit design research and the demands on system complexity are vicious, vicious things, and I made a number of painful mistakes with severe implications on yield during the first 3 years of my academic career.

Thanks to those mistakes, though, I have learned so, so much more than I thought I would during this trek, and I value and hold each of them immensely. I am truly indebted to my advisor, Ken Shepard, for giving me the latitude, encouragement and the resources to make these priceless mistakes. Through them, and the environment that Ken and his administrative team break their backs daily to keep going, I have developed an expertise at Columbia that I have no regrets about. Thank you, Ken.

The Bioelectronic Systems Lab and its myriad CAD, assembly, and measurement tools have been an outstanding technical playground for my academic experience, with all credit due again to Ken, Ria Miranda, Jason Ray, Tracey Peterson, and Helen Chong throughout the years. Beyond that, my colleagues in the lab have helped greatly to shoulder parts of my burden during my time at Columbia. In particular, Siddharth Shekar, Girish Ramakrishnan, Adrian Bradd, Michael Lekas, Fengqi Zhang, Steven Warren, Tiago Costa, Peijie Ong, Tarun Chari, Rizwan Huq, Esha John, Boyan Penkov, and Cheng Tan provided invaluable camaraderie, generosity of time and
resources, and insight into problems both personal and technical. I could not have done this without you all, and you have my most sincere thanks. (Many of the schematics in this work were made with Sid’s excellent tool YCircuit.) Fengqi especially was of great value to this work, and his support in the time leading up to the deposit of this thesis greatly eased the entire process.

Additionally, Chen Shi, Jordan Thimot, Jeffrey Elloian, and John Barth have my particular gratitude for their hours spent hands-on in the office and lab, helping me finish tape-outs, prepare samples, and assemble systems.

Noah Sturcken deserves special mention for his mentorship and generosity with help on this work, which is a direct continuation of his own doctoral work. Much of this literally would not be possible without his blessing, and his genuine interest in my development has been incredibly validating and motivational for me. His team at Ferric has always been a delight to work with, and I wish especially to thank David Jew, Ryan Davies, and Mike Lekas (again) for their aid in collaborations.

Beyond the lab, I want to thank Anandaroop Chakrabarti, Ritesh Bhat, and Yu Chen for their friendship at Columbia. And of course, Elsa Sanchez, Cassandra Kokofu, and Laura Castillo in the department office were instrumental in making sure I kept getting paid and filled out the right forms year after year.

I wish to thank Professor Luca Carloni and Paolo Mantovani for all of the time they have spent on uh, problems that I caused. I owe them both a great debt of gratitude. Their insight and wisdom helped me through a number of obstacles, and I will always wish I could have done more for them while at Columbia.

I further thank Luca, along with Matthias Preindl, Mingoo Seok, and Charles Zukowski for their contributions as members of my thesis committee.

Many people at IBM have been very generous to me, and my collaborations and internship
with teams from IBM were a real highlight of my learning experience. I wish to thank especially Naigang Wang, Bill Gallagher, Todd Takken, Phil Herget, Eugene O’Sullivan, Leland Chang, Bing Dang, Jae-woong Nah, and Paul Andry.

Professor Toby Cumberbatch helped start this whole thing going, 10 years ago at Cooper Union. I don't know what trajectory I might have had without his guidance and friendship, but I'm pretty darn fond of this one that I’ve ended up on.

Without Toby, I wouldn't have met Andrew Leader, who has been a wonderful, supportive friend for what feels like forever (in a good way). I thank him, Jennifer Wu, Muneeb Hai, Gabe Kooreman (who both are also in my life by way of Toby), Michael Nardone, Kaitlin Chou, and Kevin Tulod for their support and distractions during this part of my life. My whining will finally change topics!

Without Andrew, I wouldn't have met Alice Shen, whose love, encouragement, and partnership has kept me going through the most annoying, stressful, and anxious of times. She and my family mean the world to me. Alice, Mom, Dad, Ethan: this thesis is part of your story too. Thank you for everything.
Introduction

Power electronics has failed to evolve in performance and density in step with complex systems-on-chip (SoCs), which have benefited directly from Moore's law scaling, due to both the extrinsic limits of I/O voltage supplies and the lack of scalable magnetic technologies. This phenomenon is well-known in the power community; plenary talks and rap sessions at APEC regularly feature comments from industry experts describing power as the laggard member of the electronics family. One example cites a design in 2003 supplying 65 W at 87.3% full load efficiency over 10.1 cubic inches, compared to a design in 2013 supplying 60 W at 89.1% full load over 9.6 cubic inches [1] – not meaningfully different! Within the broader field, general attention has thus turned to pushing system complexity by leveraging Moore's law to realize significantly more complex control schemes and distributed system architectures. In conjunction with this, 3D packaging, wide bandgap semiconducting materials, and new magnetic designs continue to open possibilities for real paradigm shifts for power electronics.

As the adage goes, though, if these paradigm shifts were simple, we would have made the jump long ago. Though the incremental cost of complexity in the control architecture is lower than it has even been before thanks to Moore's law, the barrier to entry involves deploying a mixed-signal engineering team with deep familiarity with digital systems. 3D packaging for
these modules remains costly and immature, as do SiC and GaN, the most popular wide bandgap materials in this space. Finally, fundamental magnetic design has largely been sidelined in favor of continued active device and circuit topology exploration [2]. As a result, even the near-term evolution of power electronics still does not have a well-defined direction – excitingly so!

One sub-niche within bleeding-edge power electronics design concerns itself with use of thin-film magnetic inductors as a stepping stone to eventual deployment of these inductors on the same silicon die as that where the converter front end, and possibly the load are located, in an example of an extreme point-of-load (PoL) step-down deployment. The trend of high-performance processor and system-on-chip (SoC) module loads is to become ever more power-hungry, and so it becomes no longer tenable to countenance placement of the bulk of power delivery system off-module, and indeed, off-chip.

The inductors that enable this extreme PoL integrated converter architectures are not quite a result of material development, but rather of significant processing development, and represent a logically sensible but difficult to engineer next step in the evolution of PoL converters. Through early access to this technology, this work takes a modest look at changes in design methodology, intent, and intuition that are necessary for successful heterogeneous design with these thin-film inductors. Experimental results for compact package-integrated example modules are presented and discussed in light of the new perspectives brought up in this work.

Though the fundamental multi-phase buck converter structure in the example modules is exceedingly well-understood (if controversially popular – see [3,4]), the larger control architecture surrounding it contains much room for further investigation, especially when non-linear control methods are deployed. This work also takes a deep look at the behavior of a relatively old bang-bang non-linear scheme, but through the lens of sliding-mode control, a powerful framework for dealing with these classes of non-linear control systems. Though the use of sliding-
mode (or more generally, variable-structure) control in power electronics is not perhaps new [5],
a deep analysis of this specific structure appears not to have been performed prior to this work.

This work is relatively cross-disciplinary, but I have framed it from the lens of a system des-
igner with experience in transistor-based circuits, and the focus of the background material of
each chapter is chosen accordingly. Chapter 1 will seem to take an oddly long time to get the
point if one is already an expert in magnetic materials, for instance.

Chapter 1 provides an introduction to magnetic materials as pertains to the construction of
inductors, and surveys the landscape of CMOS-integrable power inductors at the time of writing.
An extended look at power dissipation in these inductors versus that in magnetic inductors more
traditionally deployed in discrete or less aggressively package-integrated systems is presented,
and a perspective of analysis considering total harmonic distortion is briefly described.

Chapter 2 shifts focus from thin-film inductors to control of buck converters. Traditional lin-
ear techniques are introduced, but the majority of the chapter is dedicated to a state-space/variable-
structure perspective, and to sliding-mode control and the very specific mindset needed to apply
it to the buck converter in a straightforward way. Stability of an indirect-sensing bang-bang con-
troller and a scheme for operating it with fixed switching frequency is analyzed and discussed.

Chapter 3 tackles the more practical aspects of unifying the previous work through packag-
ing, and looks at packaging techniques that can be used to unite these thin-film inductors with
controller front-ends, as well as some outstanding issues that seem beyond the realm of solving
in academia. In this chapter, experimental results from test modules integrating two different
types of thin-film inductors are provided.

Finally, we conclude the work with summary remarks and discussions of future work.
Chapter 1

CMOS-Compatible Power Inductors

The heart of the paradigm of switching DC-DC conversion is energy storage. Ultimately, conversion involves delivering energy unto some sort of storage element at some predetermined voltage and extracting it at some other voltage level. If the energy storage elements are lossless and the delivery/extraction networks are also lossless, then no power is lost in the intervening conversion circuitry. Of course, departures from this ideal are many and varied; exploration thereof in the context of integrated voltage regulators forms the bulk of this work.

Switching regulation must be contrasted with linear regulation or regulation with a breakdown diode, which achieve a constant output voltage by dropping the excess voltage across some lossy circuit element. Indeed, all linear regulators may be conceptualized as an implementation of a resistive voltage divider, where the low-side time-varying resistor represents the load, and where a variable high-side resistor is adjusted in time such that the low-side voltage remains at a desired value. For this reason, the ideal efficiency of a linear regulator is equal to the conversion ratio of the regulator [6].
1.1 Switched-Inductor Converters

Most generally, ideal switching converters may be conceptualized as linear, time-varying (LTV) systems whose *topological structure* changes as a function of time. At any point in time, however, the structure consists of linear elements only. As such, the underlying system equations take the form of first-order differential equations, almost always with time-varying coefficients. In the ideal framework we begin to consider here, the following assumptions are taken:

- Inductors and capacitors have no associated parasitics.
- Switches have no on-resistance or off-conductance.
- Switch states may be changed with no energy cost.
- The load may be represented as a resistor.
- The input fixed-voltage power source has no associated Thévenin resistance.

We also restrict our discussion here to non-isolated converters: topologies involving transformers and/or where significant energy is stored in coupling fields will not be considered. Additionally, switches will always be realized as at least two-quadrant switches, such that the only converters of interest as synchronous, and we do not consider operation in discontinuous conduction mode. Finally, this chapter focuses on steady-state operation of the converter.

**General Operating Principles**

The simplest (and indeed, majority of) switched-inductor converters alternate between two structures: one where an input voltage source $V_{in}$ energizes a passive network containing some number of reactive elements, and one where the input voltage source is disconnected and the
energy stored in the reactive network incites some sort of zero-input, non-zero-state response. Here, we consider the load to be embedded in the passive network.

The role of the reactive elements in the passive network is to act as a filter through their energy storage properties. The nature of this filtering is difficult to explain in a concise, elegant manner for the generic switched-inductor converter, as they are governed in general by systems of linear differential equations with time-varying coefficients. Such systems do not necessarily possess a closed-form description of the steady-state output voltage, but we may make some sundry observations about aspects of the system trajectory that allow us to confirm filtering behavior.

Switched-Inductor Converters as Filters

In the case of the buck converter, it is easy to re-cast the system as an LTI system driven by a time-varying forcing function, in which case one may use input-output transfer function theory to elucidate the filtering behavior of the system. Further discussion and justification will be provided in section 2.1.

Figure 1.1: The ideal boost converter

---

This of course explains the tendency for introductory works on the topic to use time-domain analysis supplemented with aggressive assumptions to derive interesting elementary results for switched-inductor converters.
In the case of the boost converter (figure 1.1), the system equations may be described as:

\[
\frac{d}{dt} \begin{bmatrix} V_{\text{out}} \\ i_L \end{bmatrix} = \begin{bmatrix} -\frac{G}{C} & \frac{k(t)}{C} \\ \frac{k(t)}{L} & 0 \end{bmatrix} \begin{bmatrix} V_{\text{out}} \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} V_{\text{in}} \quad (1.1.1a)
\]

\[
y = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} V_{\text{out}} \\ i_L \end{bmatrix} \quad (1.1.1b)
\]

Here, we employ dot notation to indicate differentiation with respect to time. Note that this system is second-order. \(k(t)\) encodes the switching behavior and generally only needs to be constrained to only take on either 0 or 1 as its value in order to describe all possible schemes for driving the boost converter. However, that degree of flexibility is not particularly helpful here. Let us assume a fixed, known switching frequency and duty cycle for \(k(t)\), such that \(k(t)\) is a pulse waveform.

Due to the time-dependence of \(k(t)\), there is no straightforward way to determine the state trajectory of the system, nor talk about a single ‘switching input’ that is being filtered by the system. However, if we assume that a periodic steady-state trajectory of the system exists, we can expand the quantities of interest using Fourier series and consider the impact of the component values and the switching frequency of \(k(t)\) on the Fourier coefficients. We make the strong assumption that for all waveforms of interest, there exists a Fourier series that converges absolutely to said waveform of interest. For convenience, we also assume that all waveforms are of bounded variation.

We use the complex exponential form of the Fourier series here. We denote the \(n\)th Fourier coefficients of our periodic waveforms of interest using a hat and an additional subscript, such
that:

\[ V_{\text{out}}(t) = \sum_{n \in \mathbb{Z}} \hat{V}_{\text{out}, n} e^{jn\omega_0 t} \]

\[ i_L(t) = \sum_{n \in \mathbb{Z}} \hat{i}_{L, n} e^{jn\omega_0 t} \]  \hspace{1cm} (1.1.2)

\[ k(t) = \sum_{n \in \mathbb{Z}} \hat{k}_n e^{jn\omega_0 t} \]

Note that \( k(t) \), being a pulse waveform, has Fourier coefficients given by:

\[ \hat{k}_n = \frac{\sin \left( n\omega_0 \frac{DT}{2} \right)}{n\pi} \]  \hspace{1cm} (1.1.3)

Elucidating some sort of dependence of the Fourier coefficients on the switching frequency \( \omega_0 \), \( L \), and \( C \) will help inform the claim that the boost converter structure attenuates the high frequency content introduced by \( k(t) \). First, recall that the Fourier series of a product of waveforms \( z(t) = x(t) y(t) \) has coefficients:

\[ \hat{z}_n = \sum_{m \in \mathbb{Z}} \hat{x}_m \hat{y}_{n-m} \]  \hspace{1cm} (1.1.4)

The above may be recognized as a convolution sum. The describing equations are now:

\[ V_{\text{in}} - \sum_{n \in \mathbb{Z}} \sum_{m \in \mathbb{Z}} \hat{V}_{\text{out}, m} \hat{k}_{n-m} e^{jn\omega_0 t} = L \sum_{n \in \mathbb{Z}} jn\omega_0 \hat{i}_{L, n} e^{jn\omega_0 t} \]

\[ \sum_{n \in \mathbb{Z}} \sum_{m \in \mathbb{Z}} \hat{i}_{L, m} \hat{k}_{n-m} e^{jn\omega_0 t} = C \sum_{n \in \mathbb{Z}} jn\omega_0 \hat{V}_{\text{out}, n} e^{jn\omega_0 t} + G \sum_{n \in \mathbb{Z}} \hat{V}_{\text{out}, n} e^{jn\omega_0 t} \]  \hspace{1cm} (1.1.5)
We may perform coefficient matching of the $e^{j\omega_0 t}$ terms and observe that:

$$
\hat{V}_{\text{out},n} = \frac{\sum_{m \in \mathbb{Z}} i_{L,m} \hat{k}_{n-m}}{G + jn\omega_0 C}
$$

$$
i_{L,0} = \hat{V}_{\text{out},0} G
$$

$$
i_{L,n} = \frac{-\sum_{m \in \mathbb{Z}} \hat{V}_{\text{out},m} \hat{k}_{n-m}}{jn\omega_0 L} \quad \text{for } n \neq 0
$$

Combining the above equations and taking the modulus yields:

$$
|\hat{V}_{\text{out},n}| = \frac{1}{|G + jn\omega_0 C|} \left| \hat{V}_{\text{out},0} G + \sum_{m \in \mathbb{Z} \setminus \{0\}} \sum_{l \in \mathbb{Z}} \frac{j\hat{V}_{\text{out},l} \hat{k}_{m-l} \hat{k}_{n-m}}{m\omega_0 L} \right|
$$

(1.1.7)

We may immediately see now the fundamental difficulty with exact analysis of these systems: each Fourier coefficient in fact depends on all Fourier coefficients such that an explicit solution is not possible. However, to make a statement about attenuative behavior, we only need to bound the coefficients and consider how the quantities of interest affect the bounds.

Application of the Cauchy-Schwartz inequality (equivalent to the triangle inequality in this context) and substitution of the explicit expressions for $\hat{k}_n$ yields:

$$
|\hat{V}_{\text{out},n}| \leq \frac{1}{|G + jn\omega_0 C|} \left| \hat{V}_{\text{out},0} G + \sum_{m \in \mathbb{Z} \setminus \{0\}} \sum_{l \in \mathbb{Z}} \frac{|\hat{V}_{\text{out},l}| \sin((m-l)\omega_0 DT_0) \sin((n-m)\omega_0 DT_0)}{m\omega_0 L\pi^2|m||m-l||n-m|} \right|
$$

(1.1.8)

$$
\leq \frac{1}{|G + jn\omega_0 C|} \left| \hat{V}_{\text{out},0} G + \sum_{m \in \mathbb{Z} \setminus \{0\}} \sum_{l \in \mathbb{Z}} \frac{|\hat{V}_{\text{out},l}|}{m\omega_0 L\pi^2|m||m-l||n-m|} \right|
$$

(1.1.9)

$$
\leq \frac{1}{|G + jn\omega_0 C|} \left| \hat{V}_{\text{out},0} G + \sum_{m \in \mathbb{Z} \setminus \{0\}} \left( \frac{1}{|m-n|^2} \sum_{l \in \mathbb{Z}} \frac{\text{var}(V_{\text{out}})}{2\pi^3\omega_0 L|m-l|^2} \right) \right|
$$

(1.1.10)

$$
\leq \frac{1}{|G + jn\omega_0 C|} \left| \hat{V}_{\text{out},0} G + \frac{\text{var}(V_{\text{out}})}{2\pi^3\omega_0 L} \sum_{m \in \mathbb{Z} \setminus \{0\}} \left( \frac{1}{|mn-m^2|} \sum_{l \in \mathbb{Z}} \frac{1}{|ml-l|^2} \right) \right|
$$

(1.1.11)

Here, $\text{var}(\cdot)$ denotes the total variation of the function. We note that both summations are
convergent and so are bounded above by some constant. Finally then, we can observe the fol-
lowing:

• The DC current drawn by the load affects the ripple bounds directly, but is only affected by
  the switching frequency and the capacitance value in a first-order sense.

• Both the capacitance and inductance value interact with the more nebulous portion of
  the bounds, which is related to the AC content of $V_{\text{out}}$ through its total variation. Indeed, if
  $\omega_0 nC \gg G$, then contribution of that term decreases in a second-order sense, that is, with
  the square of the switching frequency and with both $L$ and $C$.

• We may thus see that proper choice of the component values allows for the designer to
  meet an output voltage ripple specification by increasing the attenuation of the switching
  content at the output node. Indeed, without any restriction on the component values, the
  non-DC components of the steady-state output voltage may be made arbitrarily close to
  zero.

A more rigorous, if even more involved technique for analysis would be to generate a fun-
damental matrix for the system using numerical techniques to generate independent solutions,
and employ Floquet theory [7] to construct a closely related (that is, Lyapunov equivalent) lin-
ear, constant coefficient system which preserves system stability behavior and can be discussed
more cogently [8].

**Buck Converters**

The canonical buck converter is depicted in figure 1.2 with idealized elements. Let us assume
the existence of a periodic steady-state for the circuit. A period may be subdivided into phase 1,
wherein SW1 is closed and SW2 is open, and phase 2, where SW1 is open and SW2 is closed.
During phase 1, current is drawn into the inductor from the input power source, increasing the energy stored in the inductor. During phase 2, that energy is pulled from the inductor into the load. In the ideal inductor, energy is proportional to the square of the inductor current, and so similar comments about current also hold: the inductor current increases during phase 1 and decreases during phase 2.

**Steady-State Behavior**

To determine the dependence of the output voltage $V_{out}$ on the characteristics of the switching, a harmonic analysis of the circuit may be carried out as in section 1.1. However, the describing system for the buck converter does not possess time-varying coefficients:
As a result, we can merge \( k(t) \) with \( V_{in} \) and analyze as an LTI system driven by a periodic waveform, as in figure 1.3. By convention, we continue to treat \( k(t) \) as a pulse waveform with switching frequency \( \omega_0 \) and duty cycle \( D \).

The DC voltage across the inductor must be zero in a periodic steady-state, such that the DC component of the input source and the output (across the load conductance) must also be equal. The higher harmonics of the switching waveform do have a non-zero transmission to the output; the role of the capacitor is thus to form a classical second-order low-pass filter together with the inductor to attenuate this transmission.

![Figure 1.3: The ideal buck converter cast as an LTI system with time-varying input](image)

The DC value of the input source is exactly \( DV_{in} \), irrespective of the period \( T \). \( D \) by definition may only take on values on \([0, 1]\) such that the DC value of the output is always less than or equal to that of the input source. Hence, the buck converter realizes a step-down converter.
Alternatives for Step-Down Conversions

Buck converters have the significant advantage that they are easy to understand and to implement. When non-idealities are introduced, such as the irrecoverable energy cost of changing switch states, or losses within the inductors, the efficiency drops from the ideal 100%, but values well above 90% are achievable in modern commercial systems [9]. However, the buck converter is certainly not the only topology available for non-isolated step-down conversion. We discuss some of these alternatives here, with the caveat that this list is not meant to be exhaustive, but attempts to survey recent trends in the field.

Multi-level Buck Converters

Though not strictly distinct from conventional buck converters, the use of multi-level switches in the half-bridge merits special mention here. Multi-level switch elements were originally conceptualized for generating non-binary logic signals and were soon leveraged in the context of DC-AC conversion [10], where they are employed to generate, e.g., a three-level pulse waveform rather than the two-level square wave. They do so in a manner that decreases both switch stress and the undesired harmonic content that needs to be filtered out, relaxing the design requirements. Such a switch element would be termed, in particular, a three-level switch.

Within buck converters, the merits of the three-level switch are certainly still exceedingly relevant: if the required input voltages are high, the switch stress decrease is imperative, and decreasing the harmonic content in the inductor current and capacitor voltage architecturally allows for either component value to be decreased in comparison to a conventional buck converter order to achieve the same output. We do not go into detail here on the realizations of the switch element, but depict two popular topologies and relevant references in 1.4.

The use of three-level switches certainly introduces additional complexity into the system. It
can be seen immediately from figure 1.4 that additional switching signals are needed. While it is possible to replace some subset of the switches with diodes (as in an asynchronous architecture), fully synchronous realizations are generally preferred in the fully-integrated context for reasons of density and to decrease conduction losses.

**Soft-Switching/Resonant/Quasi-Resonant Converters**

Following the same conceptual vein as above, *soft switching* refers to a family of techniques that modifies the switching node behavior to decrease its harmonic content, but in a continuous valued sense, rather than the discrete valued sense achieved by multi-level switches [13]. Indeed, soft switching here refers to shaping the switching node waveforms so that there are no ‘hard’ edges. By way of comparison, the conventional buck converter is considered a ‘hard-switched’
Soft switching is often realized with a specially tuned resonant network at the output of the switch network that shapes the waveforms such that a) no switch is turned off when there is voltage across it, and/or b) no switch is turned off when there is current through it. Satisfying these conditions ensures that the conduction losses in the switch are minimized. However, this comes at the architectural price of increasing the ripple current, and holistic conduction losses are increased. Compare this to the hard-switching converter, where switches inevitably have non-zero voltage across and current through them, such that switch conduction losses are unavoidable [13].

An example of a soft-switched buck converter is depicted in figure 1.5a. The design of the passive waveform shaping network (indicated) requires a high degree of exactness in the component selection, which immediately poses a challenge in the fully-integrated context. Even in
a situation where component adjustment is available, tuning the network to obtain the required response requires additional insight and time post-fabrication, which further makes this scheme unattractive from an implementation point of view, if not from a figure-of-merit point of view. As a result, soft-switching converters are generally considered to be disadvantaged by their complexity [16].

Finally, conventional soft-switched buck converters are unable to operate at fixed frequency, and their conversion ratio is a very sensitive function of the switching frequency [17]. This may or may not be an issue, and modifications to achieve fixed switching frequency in certain soft-switching topologies do exist [18], but this aspect of soft switching also needs to be considered when a step-down conversion topology is chosen.

*Resonant converters* are often considered to be related to soft-switching converters, as they are often built around zero-current/voltage switching. In this class of converters, the ripple current is shaped to be a large-signal sinusoid, rather than the hard-switched sawtooth wave of conventional converters. The benefits of resonant conversion are derived from the soft-switching aspect, but so are the disadvantages: the complexity and requirements for tuning to achieve the desired resonant operation over the entire operating range represent an obstacle to deployment, and resonant converters display higher current ripple [13]. Converters deploying resonant switching sub-cells in traditionally hard-switched architectures are generally termed *quasi-resonant*, as the current/voltage waveforms of interest are not strictly sinusoidal. An example of a quasi-resonant buck converter is provided in figure 1.5b.

All that said, there is a sizable body of professionals [2–4, 19] that are proponents of soft-switching and/or resonant conversion and cite its further adoption as a natural step in the tenuous evolution of power electronics. In return for an increase in design complexity, resonant converters achieve far and away the most significant reduction in harmonic content, enabling
one or both of lower frequency operation and smaller required inductance/capacitance.

**Switched-Capacitor Converters**

In situations where deployment of physical inductors is for any reason not tenable, the inductor in the passive network may be eliminated, and the requisite attenuation can be achieved with just a capacitor. This class of SC (SC) converters, also known as the class of charge pumps, achieves voltage conversion through controlled charge transference to and from a so-called ‘flying capacitor’. Broadly, the flying capacitor has some known amount of charge $Q_f$ stored in it during one operational phase, and the converter re-distributes that charge over a known effective capacitance $C_o$ to achieve a known voltage during the second operational phase. Together with the load resistance, $C_o$ forms a first-order system that would asymptotically delay to zero stored energy over time, so these phases are repeated periodically to replenish the charge in $C_o$.

A direct comparison between switched-inductor and SC converters is a contentious one: properly, each topology has a particular niche that it performs well in. Because the use of only capacitors limits the attenuating behavior to first-order, it seems at first glance that SC converters are disadvantaged in their output ripple specifications [20], but in situations where the load power demand is relatively low, they are an extremely attractive way to realize a simple, CMOS-integrable, high efficiency DC-DC converter. In high output power settings, where the first-order system formed by the load resistor and $C_o$ has a very low time constant, existing limitations to capacitor density continue to form a barrier to adoption for fully-integrated SC converters. As a result, realized fully-integrated SC converters have relatively low power densities ($< 1 \text{ W/mm}^2$) [21]. Efforts have been made to address this using aggressively interleaved structures for ripple mitigation combined with high-density deep trench and/or ferroelectric capacitor technologies, with several demonstrations of $>85\%$ conversion efficiency with densities greater than $2 \text{ W/mm}^2$. 
in fully integrated systems [22, 23].

Additionally, one major architectural limitation of SC conversion is that the conversion ratios are fixed by $Q_t$ and $C_o$. However, configurable structures exist that effectively embed multiple charge transference paths and/or conversion stages and allow for more granular control over the conversion ratio [24–26], so this limitation is practically easy to surmount, especially given the low additional cost of complexity if the converter is already to be fully integrated in CMOS. Indeed, modern SC regulators are able to demonstrate output voltage ranges with reasonable (approx. 5% to 20%) worst-case efficiency degradation over output voltages of interest.

Where on-chip integration and fixed conversion ratio is not a concern, several commercial offerings boasting close to 100% efficiency are available. This is enabled by the significantly larger energy density of discrete capacitors vs. inductors [21]. The interested reader is directed to the product datasheets [27, 28] for examples of both the limitations and the benefits of using these topologies.

**Efficiency**

Fractional efficiency is defined as $\eta = \frac{P_{\text{load}}}{P_{\text{total}}}$, the ratio of the power delivered to the load divided by the total power consumed by the system – including the load. The ideal converter would have an efficiency of 1: the operation of the converter itself would not dissipate any power, and 100% of the power consumed from the input power source would be dissipated by the load.

Broadly, major deviations from this ideal in switched-inductor converters may be divided into two major categories:

- **Static loss** captures all loss mechanisms that cause undesired power dissipation that does not vary as a function of switching frequency. The major sources of static loss follow:

  (a) **DC conductance loss** describes the loss due to the presence of parasitic resistance in,
e.g., the switches, the conductor used to implement the inductor, and the interconnect. Note that the resistance here is assumed to be a large signal resistance constant with respect to frequency, hence the inclusion of the qualifier ‘DC’ in the name of this loss mechanism. This excludes power loss in intentional resistors.

(b) **Static bias power** describes, if present, the power needed to keep, e.g., operational amplifiers or other analogue elements in the controlling circuitry biased at the correct values. This also captures power loss in intentional resistors used in sensing networks.

- **Dynamic loss** captures, predictably, all loss mechanisms whose impact varies as a function of switching frequency. These mechanisms arise from very varied physical phenomena, and we will see in section 3.4 that they are incredibly important in fully integrated contexts.

(a) **Switching loss** covers the loss incurred by changing the state of the switches in the converter. Note that this is distinct from the loss due to a finite conductance in the switch, which would be covered under DC conductance loss above. Some amount of energy must be spent to do so, as it implies transference of information from the controller to the switch itself. When switches are realized with MOSFETs, the switching loss arises from the energy consumed in charging/discharging capacitors through non-zero resistances.

(b) **Skin effect loss** arises from the eponymous reduction of a conductor’s effective cross section due to induced electromotive forces (EMFs) within the conductor itself.

(c) **Winding proximity loss** is a manifestation of non-zero parasitic mutual inductance between the individual windings that makes up the intentional inductor and simi-
larly decreases the effective current-carrying cross-section of the conductor making up the inductor.

(d) We use the term *eddy current loss* to describe only losses due to induced currents outside of the current-carrying conductor. For instance, eddy currents induced in the magnetic core, in the substrate, or in surrounding metal will be lumped together in this framework.

(e) *Core hysteretic loss* arises if ferromagnetic materials are used in the core. In such materials, energy delivered into the material and stored in the form of flux cannot be fully extracted from the material, as non-zero energy is consumed in fully demagnetizing the core.

Further discussion of core-related losses follow in section 1.2.

### 1.2 Power Inductors

In this section, we discuss the current landscape of inductors that have been realized in a CMOS-integrated context. Though ultimately we will be using the hard-switched buck converter as our lens with which to view the performance metrics of power inductors, an understanding of available inductor realizations is a prerequisite for deploying any switched-inductor converter, whether or not it uses multi-level switches, soft-switching, etc.

In this section, an ‘inductor’ is a structure specifically built to harness Faraday’s law of induction, which hinges upon the generation of a magnetic field by a current flowing through a conductor [29]. However, we shall see that any such structure necessarily is affected by other physical laws, such that Faraday’s law of induction is not sufficient to describe the behavior of
the structure under all operating conditions. In particular, we will also need to consider the fol-
lowing effects:

- The conductor which carries current will have some Ohmic resistance.

- If there is other metal near the structure, the current flowing through the intentional in-
ductor will induce electromotive forces (EMFs) and thus currents in those other pieces of
metal. This effect is generally referred to as *mutual inductance*, and the resultant currents
thus generated are termed *eddy currents*. Indeed, as pointed out in section 1.1 eddy cur-
rents may even be generated inside the conductor, giving rise to the skin effect.

- There must also be electric fields present in the structure, and where these field lines be-

gin in the structure and terminate elsewhere in the structure, parasitic capacitances will
exist. At high enough frequencies, the behavior of these parasitic capacitances will dom-
ine the behavior of the entire structure. The frequency at which the purely inductive
and purely capacitive effects balance each other out is termed the *self-resonant frequency*
(SRF); above the SRF, the structure behaves capacitively. If we have the luxury of dealing
with a structure that may be modeled with only passive linear circuit elements, then the
SRF is the frequency at which the impedance of the structure is real. Note that multiple
resonances may exist in general; the lowest frequency of resonance is the practical one of
interest.

- The properties of the material in which the magnetic field is induced will have a significant

effect on the behavior of the structure. These effects are elucidated in section 1.2

* A *power inductor* is such a structure that is optimized for use in power electronics. As de-
scribed above, the application benefits from a larger inductance, and so power inductors should
be able to achieve high inductance densities and have high maximum current ratings. Additionally, the frequency range of use for a power inductor is quite low relative to RF inductors (though high relative to chokes); this will inform the selection of the core material and the layout of the structure to place the SRF appropriately.

Magnetic Cores

Faraday’s law of inductance holds irrespective of the material in which the current-carrying conductor is embedded. However, a suitably chosen material can act to increase the energy stored through magnetic flux in an intentional inductor. We refer to such materials in this work simply as magnetic materials. To more comfortably and consistently discuss modern inductor structures, we define briefly some terms of interest here. The reader interested in fundamental discussions on magnetism is referred to one of the several existing texts on the subject \cite{29,32}.

Fundamental Definitions

There are three vector field quantities that will be of primary importance to our discussion. Because the terminology and units around these quantities tend to vary from user to user, we re-define them here, loosely following the notation of \cite{33}:

- \( \mathbf{B} \) is termed the magnetic flux density or induction vector field, and has SI units of Teslas. When integrated over a surface of interest, we determine the magnetic flux \( \Phi \). This vector field is used to calculate the Lorentz force \cite{32} experienced by a charged particle.

- \( \mathbf{H} \) is the magnetic field, in analogy to the electric field of electrostatics, and has SI units of \( \text{A/m} \). In some contexts, \( \mathbf{H} \) is referred to as the demagnetizing field.

- \( \mathbf{M} \) is the magnetization, and is a field quantity that represents the local magnetic moment. Non-zero magnetic moment gives rise to microscopic currents due to the motion of or-
biting electrons in the material, while maintaining zero net current. If we denote this microscopic current density as \( j_M \), then \( \mathbf{M} \) is the vector field such that \( \nabla \times \mathbf{M} = j_M \). The magnetization also has units of A/m.

There is a significant amount of contention around the ‘correct’ way to conceptualize the physical relationships between these three fields; interested readers may peruse suitable references \([34, 35]\). For the purposes of the discussion here, laying out a pedagogically sensible framework is not strictly necessary, but we will state explicitly here that we will follow the tack generally chosen by engineers and consider \( \mathbf{H} \) to be the primary controllable quantity of interest, but admit the supremacy of \( \mathbf{B} \) in a fundamental sense.

Fundamentally, the magnetic flux density is governed by two of Maxwell’s equations, assuming a static problem:

\[
\nabla \cdot \mathbf{B} = 0 \quad (1.2.1)
\]
\[
\nabla \times \mathbf{B} = \mu_0 (j_e + j_M) \quad (1.2.2)
\]

Here, \( \mu_0 \) is the vacuum permeability, and \( j_e \) is the external current density.

\( \mathbf{H} \) is introduced as a quantity that is controlled by \( j_e \) only, such that:

\[
\nabla \times \left( \frac{\mathbf{B}}{\mu_0} - \mathbf{M} \right) \equiv \nabla \times \mathbf{H} = j_e \quad (1.2.3)
\]

**Descriptive Curves**

One of the most common ways to capture information about the behavior of a magnetic material is with a *hysteresis* curve, a dynamic plot relating either \( \mathbf{M} \) or \( \mathbf{B} \) to \( \mathbf{H} \). Notionally, the magnetization or induction field is being considered as a function of the magnetic field, which is in turn
controlled by some current. As a result, the $\mathbf{H}$ considered in these measurements is assumed to be the *applied* field. In the absence of applied current $\mathbf{j}$, the true $\mathbf{H}$ is not identically zero. Relevant governing equations reduce to:

$$\nabla \cdot \mathbf{H} = -\nabla \cdot \mathbf{M} \quad (1.2.4)$$

$$\nabla \times \mathbf{H} = 0 \quad (1.2.5)$$

Thus, depending on the qualities of the magnetization of the material, a non-zero magnetic field may arise even without any applied current density. It is in chiefly in these contexts that $\mathbf{H}$ is termed the 'demagnetizing field', as it acts counter to the magnetization. When an applied current density exists, then, we may partition the magnetic field as $\mathbf{H} = \mathbf{H}_a + \mathbf{H}_d$, the sum of the *applied* field and the *demagnetizing* field. In this work, we explicitly assert that the materials under investigation do not retain a demagnetizing field in the absence of applied field.

For simplicity, the measurements and presented data generally assume a one-dimensional magnetic field and induced flux density. Under these conditions, we may envision the relationship on a simple two-dimensional plot. In the rest of this work, we use 'M', 'B' and 'H' to refer to these one-dimensional quantities, which may vary as a function of time.

We mention here the concept of *shape anisotropy*, as it generally affects the structures used in thin-film inductors. Briefly, the specific shape of the magnetic material will impact the demagnetizing field present in the material, causing it to be anisotropic. This demagnetizing field due to the inherent magnetization will interfact with the applied field and give rise to different B-H or M-H curves depending on the direction in which $\mathbf{H}$ is applied [33]. In rectangular structures, one generally speaks of an 'easy axis' and a 'hard axis', the former of which has higher low-field permeability.
With these definitions in hand, we may look at candidate magnetic materials for core construction. First, let us consider abstractly what an inductor designer wants in a relationship between flux density and field strength. As asserted in equation (1.2.3) above (Ampère’s circuital law), increasing the current flowing in the conductor increases the curl of the magnetic field $H$. The magnetic flux is directly proportional to the energy stored in an inductor; if we assume a uniform cross-section for the flux lines, then the flux density is directly proportional to the same. Thus, if we wish to maximize energy storage for a given current, we would like the ratio of flux density to field strength to be large. Indeed, inductance may also be calculated as the ratio of relevant magnetic flux (not to be confused with $B$, the flux density) to the applied current, $L = \Phi / i_a$.

Physically, the mechanism of energy storage is domain alignment within the material: energy is represented by the orderedness of the material within the structure of interest. The phenomenon of an applied field being able to increase the orderedness of the internal domains of the magnetic material is also referred to as magnetization of the material. Note that the purpose of introducing magnetic material into an inductor is to increase the flux density/energy storage being induced by the field, rather than to retain magnetization when no field is being applied, as a permanent magnet would.

Sample B-H curves for Permalloy and high-purity iron are depicted in figure 1.6. Immediately, we note the following features of the curves:

- In figure 1.6a, both curves describe a one-to-many mapping that does not include the point $(0, 0)$. These were thus not taken assuming a starting stored energy of zero. The one-to-many behavior is a function of the past state of the material and describes hysteretic behavior in energy storage of the core. Curves including $(0, 0)$, often called magnetization curves, are provided in figure 1.6b for these materials.
Figure 1.6: Material descriptive curves for Permalloy
(a) The hysteretic aspect of this curve captures the core hysteretic loss described in section 1.1. Succinctly, after the energy stored (in the form of flux) becomes non-zero due to application of a magnetic field, extracting all of the energy back out is not a matter of reducing the field back to zero! Instead, the field must be moved past zero in order to reduce the flux to zero. The area of the hysteretic loop is indeed proportional to the power delivered to the inductor to magnetize it \[33\]. This power is dissipated as heat.

(b) Due to physical symmetry, the x-intercepts of a B-H curve are identical, and the magnitude of the intercept is termed the \textit{coercivity} \(H_c\) of the material under the measurement conditions. On an M-H curve, the x-intercepts are termed the \textit{intrinsic coercivity} \(H_{ci}\). These values are distinct, and in ferromagnetic materials, \(H_{ci} > H_c \[37\].

(c) Low coercivity materials are preferred for inductor construction, as they imply less core hysteretic loss. These materials are referred to as soft magnetic materials. Here, Permalloy has a low coercivity, and iron a relatively high one.

(d) Similarly, the magnitude of the y-intercepts of the B-H curve are denoted as the remanence or remanent magnetization of the material.

- At low applied fields, the B-H relationship is proportional, with \(B = \mu_r \mu_0 H\). \(\mu_0\) is the \textit{vacuum permittivity}, and \(\mu_r\) is the \textit{relative permittivity}. At high applied fields, however, the relative permittivity decreases to 1 such that the material incrementally behaves like free space and does not augment energy storage abilities of the structure. On an M-H plot, the curve would flatten to zero slope at such fields.

(a) This behavior is referred to as \textit{saturation}, as the material is considered to be ‘saturated’ with energy and no longer able to respond. Physically, the domain alignment
is at a maximum, and additional applied field does not engender an increase in order within the structure.

(b) Soft materials often displaying correspondingly ‘soft’ transitions from high relative permittivity to unity relative permittivity. High coercivity materials often display sharp, sudden transitions from the low-field permittivity down to unity.

(c) The saturation mechanism described above is sometimes referred to as *DC saturation*, as distinguished from *AC saturation*, which describes an inability for the magnetic domains to re-align with a quickly changing magnetic field. B-H or M-H curves, which generally assume quasi-static operation, are unable to capture this behavior in the material. The overall effect is similar to that in DC saturation: if the magnetic domains cannot re-align, then the flux density will not increase in a manner consistent with the applied magnetic field, and incrementally, the structure will behave as if there is no magnetic material present. This, along with the inherent finite self-resonance frequency of the structure, limit the range of useful frequency for any inductor structure.

The B-H curve of free space would display no saturation characteristics, no hysteresis, and significantly less (but non-zero) energy storage potential in the low-field operating regime. As a result, air-core inductors trade off inductance density for low loss over a wider range of currents. By way of contrast, figure 1.7 displays simulated buck converter current waveforms for an inductor with a soft-saturating magnetic core. An air-core inductor would display virtually piecewise-constant slopes. However, as the current increases in the magnetic core inductor, the incremental inductance drops, and the slope increases markedly.
Modern CMOS-Compatible Inductor Structures

In this section, we discuss examples of CMOS-integrated inductors. We restrict our detailed discussion here to only those that have been realized in a fully integrated context. Package/module-integrated examples are significantly more commercially developed, and interested readers are directed to resources describing major successful module-integration strategies [38–40].

Spiral

The planar spiral inductor is perhaps the most well-known manifestation of the integrated inductor in the general circuit design community and is a major enabler for radio-frequency integrated circuit (RFIC) systems. In such systems, the inductor generally plays a role in resonant networks or in filter structures operating in the GHz range, precluding the use of magnetic materials (cf. section 1.2). It is just as well then that the achievable inductance densities of air-core planar spiral inductors was deemed acceptable for RFIC deployments. An example structure is depicted in figure 1.8.

For power inductors intended for use in hard-switched buck converters, the inductance densities achievable by air-core planar spiral inductors are prohibitively low. In order to circumvent this, intrepid designers have experimented with adding magnetic layers above/below the planar
structure \[42\,43\], eventually leading to the yoke/stripline structures to be discussed next.

**Yoke/Stripline**

The stripline, yoke, or racetrack structure (figure \[1.9\]) consists fundamentally of a conductor clad in all directions by magnetic material to increase the energy storage due to the induced magnetic field by way of increasing the flux density. They may be considered generalizations of a magnetic-clad spiral structure and were explored significantly in previous work \[44\,46\], which demonstrated high inductance densities. In section \[3.4\] we further investigate buck converter design with yoke inductors and discuss experimental results.

Much of the previous work has focused on exploring yoke structures for power inductors due to the conceptual simplicity of the conductor construction. However, the construction of the required two magnetic layers and the magnetic vias introduces significant complexity into the overall process that has no synergy with the complexity in the CMOS copper back-end, making this structure more costly to develop for production.
There have also been efforts to realize structures with very large return current loop areas, such that the lower flux density is compensated for by a large aggregate flux \[47\]. These structures attempt to trade off density for efficiency, as the large return loop area allows removing of some or all of the magnetic cladding for the same inductance. However, engineering a larger loop area necessitates more area, and if the structure needs to co-exist with other circuitry that may interfere with the return loop, the complexity of the structural design can quickly become untenable.

**Solenoidal**

The solenoidal inductor is far and away the most popular of discrete inductor structures, and most discussions of inductor design for power applications will assume a solenoidal topology \[13\]. A current-carrying conductor is wound around a magnetic core such that the effective loop area is multiplied by the number of windings, leading to a significant increase in the flux of the structure. An additional benefit is that such a scheme allows for very flexible tuning of the flux return path, certainly compared to the yoke structure. Though we do not go into analysis of the magnetic circuit formed in these physical structures, design of the flux return path can be a very powerful tool for inductor design \[48, 49\].

In contrast to the yoke design described above, solenoidal designs in a CMOS back-end
would require two conductor layers, a conducting via layer, and only one magnetic core area.

If a copper damascene process is already being used in the back-end, however, it is not significantly more difficult to simply scale that up. An example stack-up is illustrated in figure 1.10.

With a single magnetic core structure, the use of laminations to decrease eddy current losses in these structures also becomes tenable [50, 51].

In section 3.4 we investigate buck converter design with solenoidal inductors as well.

![Figure 1.10: A stack-up for a solenoidal inductor in a CMOS back end, from [52]](image)

**Comparison of Modern Structures**

Table [1.1] summarizes several examples of recent work in on-die integrated inductors.

A few remarks on the data presented in the table:

- The inductance density is presented both over area only. Most planar inductor structures will not report density over volume, but all of these structures require extra layers in the back-end. Moreover, all of these structures will block access to top redistribution wiring or
Table 1.1: Comparison of integrated inductors

<table>
<thead>
<tr>
<th>Reference</th>
<th>Realization</th>
<th>Ind. density (nH/mm²)</th>
<th>L/R at 100 MHz</th>
<th>Peak Q</th>
<th>Frequency of peak Q (MHz)</th>
<th>DC resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>52</td>
<td>Solenoidal</td>
<td>290</td>
<td></td>
<td>10.5</td>
<td></td>
<td>4 Ω</td>
</tr>
<tr>
<td>53</td>
<td>Solenoidal</td>
<td>96</td>
<td>17.5</td>
<td>4.77</td>
<td>18</td>
<td>50</td>
</tr>
<tr>
<td>54</td>
<td>Spiral</td>
<td>30.36</td>
<td>17.6</td>
<td>27.7</td>
<td>1500</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>Spiral/Stripline</td>
<td>40</td>
<td>5</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>Spiral/Stripline</td>
<td>50</td>
<td>4</td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>Solenoidal</td>
<td>160</td>
<td>3.12</td>
<td>10</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Spiral/Stripline</td>
<td>603</td>
<td>2.39</td>
<td>1.59</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Stripline</td>
<td>51</td>
<td>1.66</td>
<td>0.45</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Stripline</td>
<td>82</td>
<td>4.2</td>
<td>1.5</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Stripline</td>
<td>260</td>
<td>7</td>
<td>3.5</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Stripline</td>
<td>200</td>
<td>7.96</td>
<td>2.39</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Spiral/Stripline</td>
<td>26.2</td>
<td></td>
<td>70</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>Spiral</td>
<td>58</td>
<td>1.33</td>
<td>1.27</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Stripline</td>
<td>24.4</td>
<td></td>
<td>11.7</td>
<td>5.5</td>
<td></td>
</tr>
</tbody>
</table>

area array I/O, just like any other passive implemented in the far back-end.

- Maximum Q (quality factor) is a misleading factor to perform comparison on, as the frequency of maximum Q is not the same from structure to structure. For that reason, we also calculate the ratio of small-signal inductance to small-signal resistance of the structure at 100 MHz where possible. 100 MHz is chosen as it is a value in the range of ‘high-speed’ switching for modern buck converters.

- Because stripline structures and spiral structures with magnetic cladding are very similar, we do not distinguish between them very strictly here. If the intention is clearly to concentrate flux \textit{radially around the conductor}, then we do note them as stripline; if the intention is to only concentrate flux in the ‘center’ of a spiral structure, then we note them as spiral. However, this is a largely semantic point.

- Information is not provided by the reporting parties for some structures, which should not necessarily reflect that the inductor would perform poorly with respect to that metric.

\textbf{Consequences of Using Thin-Film Inductors}

In order to harness thin-film inductors in buck converters, the designer needs access to large-signal-accurate models for said inductors. This is already a relatively difficult task for even discrete inductors: predictive equations such as the Steinmetz family of equations \cite{65} or models provided by vendors are limited to very specific materials and constructions, and often assume duty cycles close to 50% to simplify the task at hand \cite{66}. Such assumptions may be acceptable for designers that aim to deploy discrete converters, but since fully-integrated switched inductor regulators may be deployed in DVFS settings, an assumption of fixed or barely changing duty cycle is clearly inappropriate. In a similar vein, use of thin-film inductors implies that proper
safety margins need to be introduced into the design methodology in order to account for on-chip variability.

The most immediate distressing consequence of using thin-film inductors is the low available inductance density. Even best-in-class densities of 1.3 $\mu$H/mm$^2$\textsuperscript{67} only provide 2.6 $\mu$H over an area of, say, 2 mm – and best-in-class densities do not reflect best-in-class AC loss performance! We shall see that the primary predicted consequence to efficiency is that core losses will now become considerable, and mitigation strategies are complex.

The following subsections discuss loss mechanisms and non-linearities that apply to all inductors. We restrict the discussion to the specific manifestation in recent thin-film magnetic inductor development only. However, this is not meant to imply that the aspects therein only apply to thin-film magnetics.

**Core Losses**

As available inductance in a fixed allocated area goes down, the effectiveness of the converter structure as filter also goes down, resulting in increased high-frequency content in the output voltage and the inductor current. Critically, an increase in the high frequency content in the inductor current immediately increases loss due to several mechanisms: first, all eddy current-based effects (proximity loss and core eddy current loss) increase, as the rate of change of the magnetic field increases, thus directly increasing the magnitude of the induced EMF. Also, core hysteretic power loss increases, as the energy cost of changing the magnetization of the core must be ‘paid’ more often per unit time.

The high ripple in the inductor current is further exacerbated by the soft saturating characteristic of low coercivity materials. Under hard switching assumptions in the buck converter, the voltage across the inductor is fixed to one of two levels. As the inductor current increases, the
effective inductance of the inductor decreases, and so by Faraday's law of induction, the rate of increase of inductor current becomes even larger! Without the effects of core saturation, the ripple would be expected to increase linearly with decreasing inductance under fixed conversion ratio and switching frequency in a buck converter (see section 1.2), but with soft saturation, the increase is now super-linear in a manner highly dependent on the nature of the saturation.

**THD-Based Analysis Framework**

To allow us to draw useful conclusions about circuit design parameters, we will consider the loss holistically and in a linear fashion through its manifestation at a fixed inductor bias current as a non-zero resistance in the small-signal parameters of the effective two-port device. Both from a physical understanding of the various loss mechanisms, and from empirical measurements, we may expect this resistance to increase monotonically as a function of frequency until parasitic shunting capacitance in the layout from the input to the output dominates. This point manifests as the observed self-resonant frequency (SRF) of the inductor under consideration. Example measured small-signal AC resistance plots for an un-saturated yoke-construction device are shown in figure 1.1. As DC current increases, inductance drops directly due to the onset of saturation. However, this is accompanied also by a decrease in AC resistance, as the magnetic material participates less effectively in energy storage and thus contributes less to energy loss. A clear trade-off is thus observed: the addition of magnetic material increases inductance density, but at the cost of introducing new energy loss mechanisms that need to be taken into account during the design and specification of the inductors to be deployed in the system.

Because this work focuses on the ramifications of using thin-film integrated inductors, we are most interested in formalizing concise, clear ways to discuss the specific manifestation of the energy loss introduced by thin-film magnetics in a circuit-design-theoretic context. Such
a formalism should hold across a wide range of input voltages and conversion ratios. We may use the total harmonic distortion (THD) of the inductor current waveform in order to capture succinctly the relative contribution of the non-DC inductor loss to the absolute power loss. Here, we use the usual fundamental THD definition:

\[
\text{THD}_f = \sqrt{\sum_{n=2}^{\infty} \frac{V_n^2}{V_1}}
\]  

(1.2.6)

\(V_n\) refers to the nth harmonic of some waveform \(V\) expanded assuming a known fundamental frequency \(f\). In subsequent references to this quantity, we will always assume that \(f\) is the switching frequency of the converter (or sub-converter, in the case of a multi-phase system), and so, we denote \(\text{THD}_f\) as just ‘THD’. THD is employed often in contexts where linearity needs to be characterized, such as amplifier chains in communications systems. Traditionally, THD in the context of power systems is largely employed in alternating current systems deployed in power transmission or in motor drives [68], where there exist fixed transmission frequencies with respect to which harmonic distortion needs to be minimized below a certain specification.

In the case of the DC-DC converters under investigation in this work, THD is not an imme-
diately natural metric to use in considering the behavior of the system, since there are no wave-
forms (current or voltage) in the system with a single-tone characteristic under ideal switch/ideal
inductor operating conditions. Within the study of buck converters, THD has only been used to
address winding proximity loss in conjunction with Fourier analysis, but even then, it has yielded
insightful design constraints for winding spacing when performing discrete inductor design [69].

The current through the inductor under the aforementioned conditions is easily determined
to be an asymmetric triangle wave [13], and so a quantitative comparison is easily made between
the (non-zero) THD of the ideal asymmetric wave and the waveform under observation in the
non-ideal system. It will be demonstrated below that such a comparison, along with suitable ob-
servations of relative amplitudes between the ideal/non-ideal waveforms, allows for informed
commentary on and explanation of phenomena observed in efficiency curves taken from hard-
ware measurement.

We restrict our analysis here to a comparison of non-ideal waveforms to that of a similarly
parametrized system running in forced continuous conduction mode with no non-DC loss. The
THD of the zero-coupling, zero-non-DC loss system is hereafter referred to as the ‘baseline’ THD.
The baseline inductor current THD of a single-phase system can be calculated exactly using the
closed-form Fourier series for the asymmetric triangle waveform characterizing the steady-state
inductor current in the ideal single-phase switched-inductor buck converter of figure 1.2.

Effects of Duty Cycle

A closed-form expression for one period of the steady-state non-DC portion of the inductor cur-
rent as an asymmetric triangle wave is straightforward to state. Without loss of generality, we
define the current at time 0 as 0 A, such that the resulting function is odd. Then, the steady-
steady non-DC inductor current, normalized to unity amplitude, is:
A representative period is plotted and annotated with the symbols of interest in figure 1.12. It is important to note that the peak-to-peak amplitude of the asymmetric triangle wave, $2I_{pp}$, depends on the input voltage and the duty cycle, as indicated in equation (1.2.8). We discard that information implicitly during the calculation of THD (equation (1.2.6)) in any case, but highlight it explicitly here to call attention to the extra information that is lost, since the amplitude information will also be of importance when discussing overall efficiency as a function of switching frequency.

Because this waveform is odd and centered about zero, it may be represented as an infinite
series of scaled sine functions only, through a Fourier series expansion [70]:

\[
\frac{i_{L,\text{non-DC}}(t)}{2I_{pp}} = \sum_{n=1}^{\infty} b_n \sin \frac{2\pi nt}{T} \tag{1.2.9}
\]

\[
b_n = \frac{2(-1)^n}{(\pi n)^2 D(1-D)} \sin (\pi n (1-D)) \tag{1.2.10}
\]

The normalization of the waveform ensures that Fourier coefficients are a function of duty cycle (or equivalently, conversion ratio) only. With this expression, we may plot the baseline THD for the ideal inductor current as in figure 1.13. The baseline THD for a single-phase inductor system varies strongly and symmetrically with duty cycle: at 50%, the baseline THD is 11%, but as the duty cycle changes in either direction, the THD increases monotonically, indicating that relatively more high frequency content is introduced into the system. Indeed, at very low and very high conversion ratios, the THD may exceed 100%. This indicates in a transparent, straightforward way that converters operating at either very high or very low conversion ratios contain significant energy in higher loss operating frequencies of the device, relative to the fundamental component.

![Figure 1.13: THD vs. duty cycle for an ideal buck converter](image)

A final complicating factor is the relatively low saturation current limit available in thin-film inductors, generally less than 400 mA. Though DC saturation may be largely mitigated using
inversely coupled inductors [59], AC saturation (as discussed in section 1.2) can very adversely affect both the amplitude of the fundamental and the THD of the inductor current, further increasing power loss.

**Effects of Switching Frequency**

Increasing switching frequency has the immediate consequence *with respect to inductor-related losses only* that eddy-current related losses go up, but the inductor current high-frequency components decrease. With this, the high-frequency components of the magnetic field decrease as well, and so core hysteretic losses also decrease. In more traditional operating regimes for buck converters, core losses are largely ignored [13], and so the conventional wisdom is that increasing switching frequency strictly increases loss, so long as the skin effect is negligible at the frequency of interest.

Moreover, the quality factor $Q(\omega) = \omega L(\omega) / R(\omega)$ evaluated at the switching frequency has been viewed as a major figure of merit for inductors in general, including those deployed in switched-inductor converters [50]. In light of the above analysis, we may see that this is only approximately true, since at least 11% of the non-DC power is not at the switching frequency in the baseline case. In the presence of strong non-linearities and at duty cycles close to 0 or 1, a significant amount of the non-DC power will be at frequencies above the switching frequency, implying that $Q(2\pi f_{sw})$ is a significantly incomplete descriptor of the inductor performance within the system under consideration. It is also true that quality factor fails to accurately represent holistic switched-inductor system performance at operating points where the DC currents are high, and DC power consumption in the load dominates the efficiency calculation.
Remarks

As can be inferred from equation (1.2.8), the fundamental component itself also varies strongly as a function of several core operating parameters for a switched-inductor buck converter: switching frequency, conversion ratio, input voltage, and inductance value. This points out an immediate additional problem with naively using Q as a metric for power inductor quality: in operating conditions where THD is high, Q underestimates the overall loss in the inductors. In systems using non-linear thin-film inductors, high THD with a low fundamental component is well within usual operating parameters. Again from equation (1.2.8), it is clear that decreasing the inductor ripple by increasing the inductance or the switching frequency decreases the amplitude of the fundamental component without affecting THD. Decreasing the input voltage while maintaining a fixed conversion ratio also has the same effect. However, the conversion ratio $D$ is observed to play a role in both the normalized amplitude of the fundamental and in the peak-to-peak inductor current ripple, as seen in figure 1.14 which depicts both the normalized fundamental amplitude and the peak-to-peak inductor current, each relative to their global maxima at a conversion ratio of 50%. Both amplitudes drop as operation moves away from the 50% conversion ratio point, implying that Q, and especially peak Q, is an unsuitable metric for global switched-inductor buck converter operation with these thin-film devices: the target conversion ratios are of significance as well.

As the amplitude of the fundamental decreases, it may have seemed heretofore intuitive to claim that AC loss decreases directly with it. However, it is clear now that the complexities of AC loss imply that this is not strictly true, especially if the mechanism of decrease of the fundamental amplitude involves an increase in THD. Indeed, if the fundamental is sufficiently close to the corner of the increase in resistance, an increase in THD may shift significant energy to high resistance operating frequencies of the device. This effect is most significant where THD is observed
Figure 1.14: Fundamental amplitude assuming constant peak-to-peak ripple and peak-to-peak inductor current to increase quickly, and is easily quantified by considering the derivative of the THD, plotted also in figure 1.13. It may be observed that this point of maximum THD change occurs around the maximum ripple 50% duty cycle operating point, which implies that for converters that do not operate at a single conversion ratio, particular attention needs to be paid to the efficiency curves in order to maximize efficiency over all operating regimes.

Figure 1.15 further reinforces these ideas, but from the perspective of operating frequency: at low frequencies, the overall ripple is large in an ideal air-core inductor fundamentally, however, in the presence of a soft-saturating magnetic core, the ripple increases super-linearly with decreasing saturating frequency once below a knee point. Above a critical frequency (approx. 70 MHz, in this simulation), the ripple is kept low enough to cause the THD performance to flatten out. Note that the THD, however, is still slightly greater than the ideal 11% at 50% duty cycle.
Figure 1.15: THD and fundamental component magnitude in simulated buck converter run at 50% duty cycle, deploying a soft-saturating inductor
Chapter 2

Control of Buck Converters

It is important not to lose sight of the ultimate engineering objective of this entire exercise, which is to create a true voltage source of prescribed value. As will be discussed in this chapter, the buck converter as described above, even in the ideal case, only achieves this goal if the load is fixed with respect to time. If constant parasitic resistance is allowed for in the inductor, the buck converter never is able to achieve that goal. The task at hand is now one of system design: given some plant, that is, the buck converter, how can we shape its behavior to achieve the desired system behavior?

In this chapter, we consider basics of linear control methods in order to fully acquaint the reader with concepts and, more importantly, limitations around the use of linear control. This is not to downplay the importance of these methods, but to highlight the improvements (and indeed, deficiencies) afforded by use of non-linear control methods for these systems.

This section assumes familiarity with state-space theoretic methods for system analysis. Interested readers are referred to one of the many references on the topic [8, 71].

1I will prefer to use terminology from broader engineering notions of control theory in this thesis, as it draws a closer analogy to the exceedingly wide body of work available in, e.g., the chemical and mechanical engineering fields.

2Un-interested readers are strongly encouraged to look at the references anyway.
2.1 Formulating LTI Approximate Systems

Let us begin by stating a relatively easy-to-understand problem: given the buck converter structure discussed in the chapter above, how can we architect some control architecture that causes the output characteristic to be controlled to a constant value even with disturbances from a time-varying load resistance? Failing that, how well can we do? This is of course a familiar problem to any student of control theory, and any engineer with a few years of training should be able to suggest, at least notionally, the use of feedback.

We will use the following notation to consider the systems of interest in this chapter:

\[ \dot{x}(t) = A(t)x(t) + B(t) + u(t) \]  
\[ y(t) = C(t)x(t) + E(t) + u(t) \]

\( x(t) \) represents the state vector, \( u(t) \) the input vector, and \( y(t) \) the output vector. In much of the subsequent discussion, the exact nature of the output is unimportant, and we will be largely concerned with the first of the above equations.

Furthermore, we formally define feedback here as a modification to the system structure that involves introducing dependence of any portion of the system on any number of outputs or states. This is a very vague definition, but does not limit us to discussion of, say, LTI systems.

An immediate roadblock now appears: due to the presence of the time-varying switch components, implying a time-varying \( A(t) \), there is no intuitively clear path forward for designing these systems to have the required behavior and for understanding what the design space for the controller might look like. The treatment of the boost converter, a relatively simple converter, in section 1.1 highlights how generally intractable dealing with the underlying system can be.
The historical tackling of this problem hinges on some form of time-averaging being introduced into the system such that the system is transformed (in an approximate way) from an LTV system to some sort of nominally equivalent linear time-invariant (LTI) system. In the desired approximate system, $A$ is constant, rather than time-varying. Within the correct confines, this family of techniques can be exceedingly useful, as they allow use of transfer function analysis, which is immediately more familiar to the majority of circuit designers. Under an LTI assumption, the buck converter now may be described with several transfer functions\(^3\), each of which may be designed and modified accordingly. The most important of these transfer functions are:

- the driving-point output impedance, $\frac{V_{\text{out}(s)}}{I_{\text{out}(s)}}$
- the line-to-output transfer function, $\frac{V_{\text{out}(s)}}{V_{\text{in}(s)}}$, where $V_{\text{in}}$ is the supplied voltage, and
- the control-to-output transfer function, e.g, $\frac{V_{\text{out}(s)}}{V_{\text{ctrl}(s)}}$ or $\frac{V_{\text{out}(s)}}{D_{\text{ctrl}(s)}}$. $V_{\text{ctrl}}$ is the setpoint for the output voltage, and $D_{\text{ctrl}}$ is the duty cycle of the signal driving the switches.

The latter representation is especially popular when PWM control is used explicitly; the exact choice depends on the control system deployed.

- Depending on the system deployment, the driving-point input impedance $\frac{V_{\text{in}(s)}}{I_{\text{in}(s)}}$ may also be relevant for ensuring that the power factor of the converter subsystem is within specification\(^{13}\).

Here, we provide some introductory details concerning averaging towards approximating the system as time-invariant, and the subsequent need for linearization.

It is widely agreed that all averaging techniques are equivalent, resting ultimately on recognition of the time-varying switching network as problematic, and then performing averaging.

---

\(^3\)As elegant as having a single MIMO system description in state-space can be, the notion of having to learn a whole new formalism for system analysis turns many people off of it, which is an undeniable downside. Circuits are more naturally simulated (e.g, from the cockpit of Virtuoso) on a nodal voltage or branch current basis, as opposed to on a state basis, as well, so shoehorning everything into the transfer function framework in intuitively appealing.
over a period to eliminate switching harmonics, thus establishing a time-invariant system \[72\]. Post-averaging, though, the system may not be linear: even after \(A(t)\) and \(B(t)\) are rendered time-invariant, it is often the case that they will have dependence on the state variables, especially in a system under feedback control. The example of the current-mode controlled converter topologies is a classic example, and will be discussed in section 2.2. Therefore, equations (2.1.1) should not be taken to imply linearity of the underlying system, and do not represent a unique set of descriptive equations for the system. Indeed, many converters are not truly linear, but are bilinear \[74\]. Following averaging, then, standard linearization/small-signal analysis techniques \[75\] are used to linearize any non-linear features of the system to yield an LTI system for analysis.

This technique has a very strong caveat associated with it: under such assumptions, we are claiming that the switching action of the system does not affect the dynamics of the system at all. Even if we assume dynamics of interest all occur ‘significantly below’ the switching frequency, this claim does not hold up under rigorous examination. Presentations of averaging techniques must also come with discussions of the frequency ranges over which one may expect the approximate system to be accurate at.

Moreover, though the averaging techniques are equivalent, certain classes of control (notably peak-current control) define the duty cycle implicitly, and opinions differ on tractable approximations that allow the duty cycle to be expressed as a function of the state variables in order to linearize the system. Indeed, some approximations hide problematic behavior in those those systems \[76\]. That said, the usefulness and applicability of this technique has been discussed at length in the literature \[13\], and extended techniques to deal with perceived inadequacies continue to be a rich research subject.

As an example of averaging, let us consider the state-space averaging formalism \[77\] as applied to the boost converter and contrast it with the full harmonic balance expansion performed
in section 1.1. We will only consider the averaging of the $A$ and $B$ matrices here, starting from the equations of (1.1.1). We note that $k(t)$ takes on the value 1 for $D \times 100\%$ of the period, and the value 0 for $(1 - D) \times 100\%$ of the period. We thus use a piecewise representation over one period:

\[
\dot{x} = \begin{bmatrix}
\frac{-G}{C} & \frac{1}{C} \\
\frac{-1}{L} & 0
\end{bmatrix} x + B V_{\text{in}} \equiv A_1 x + B V_{\text{in}} \quad \text{for } 0 \leq t \leq DT \tag{2.1.2}
\]

\[
\dot{x} = \begin{bmatrix}
\frac{-G}{C} & 0 \\
0 & 0
\end{bmatrix} x + B V_{\text{in}} \equiv A_2 x + B V_{\text{in}} \quad \text{for } DT \leq t \leq T \tag{2.1.3}
\]

Note that $B$ is already time-invariant in this system, and appears identically in both sub-representations. A new set of equations is now constructed using the weighted average of the $A_x$ matrices above:

\[
\dot{x}_a = D A_1 + (1 - D) A_2 + B V_{\text{in}} \tag{2.1.4}
\]

Should $A_1$, $A_2$, or $B$ be non-linear in $D$, the resultant set of equations will need to subsequently be linearized in order to apply LTI techniques.

Again, owing to the structure of the buck converter, the $A$ matrix is time-invariant even before averaging, which suggests the semantic re-casting of the input as $k(t) V_{\text{in}}$ in order to allow us to work with an LTI system with no loss of accuracy.

### 2.2 LTI Control Design

Once time-averaging and linearization have been performed and the system-under-analysis is approximable as an LTI system, standard methods may be employed to shape the overall transfer function as desired. Here, we briefly describe two major types of feedback structures employed in the LTI-approximation framework.
Voltage-Mode Control

Voltage-mode control is perhaps the most straightforward scheme to understand for those circuit designers already notionally familiar with feedback: the control input is made a function of a direct measurement of the output voltage, generally made with some sort of shunt sampling structure. Through shunt sampling, the output impedance is decreased by the loop gain $T(s)$. The loop gain is shaped using the usual transfer function-based techniques to ensure sufficiently stable behavior.

A realization of voltage-mode control is depicted in figure 2.1. The PWM block converts a compensated-version of the voltage-domain error signal $v_e$ to a PWM wave switching from 0 to $V_{in}$. With this structure, the transfer functions of interest become:

$$T(s) = \frac{V_{ref}H(s)}{DV_{in}} \left( \frac{1}{1 + sLG + s^2LC} \right) \quad (2.2.1)$$

$$\frac{V_{out}(s)}{I_{out}(s)} = \frac{sL}{1 + sLG + s^2LC} \left( \frac{1}{1 + T(s)} \right) \quad (2.2.2)$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{D}{1 + sLG + s^2LC} \left( \frac{1}{1 + T(s)} \right) \quad (2.2.3)$$

$$\frac{V_{out}(s)}{V_{ctrl}(s)} = \frac{T(s)}{1 + T(s)} \quad (2.2.4)$$

Note that without feedback, the second order characteristic equation implies a system $Q$ of $R\sqrt{C/L}$. Practically, this will be always above $1/\sqrt{2}$, implying that the open-loop transfer functions exhibit peaking in magnitude accompanied by a $180^\circ$ shift in phase at resonance. Proper design of $T(s)$ allows for this to be reshaped accordingly.

---

4 For those unfamiliar with two-port feedback terminology, see the excellent description in [78].
5 Because this work focuses on state-space analysis, we do not formally define loop gain here; we follow the terminology of [79], in general.
6 Not to be confused with the inductor quality factor $Q$. 

Current-Mode Control

Current-mode control is not, as the name and analogy to voltage-mode sampling might imply, simply using series sampling instead of shunt sampling in a single feedback loop. Rather, current-mode control performs series sampling of the inductor current in one minor feedback loop that aims to control the inductor current to some fixed level $I_{ctrl}$, but also performs shunt sampling of the output voltage in a major feedback loop to control $I_{ctrl}$ such that the desired output voltage is maintained. Ultimately, any linear feedback scheme using high loop gain needs to perform shunt sampling in order to realize a low output impedance, which is necessary for DC-DC converters.

Current-mode control can be further sub-divided into schemes that control the average inductor current, the peak inductor current, or the valley inductor current. A realization of peak current-mode control is depicted in figure 2.2. Here, $v_{iL}$ represents an ideal measurement of the inductor current transformed into the voltage domain. The PWM block now has a more complicated function: regardless of its past state, it will switch to delivering $V_{in}$ at its output every $T$ seconds. However, when $v_{iL}$ is greater than a compensated version of $v_e$, the PWM block will deliver 0 at its output. In this way, fixed-frequency operation is achieved. Transfer functions of interest here are less straightforward to describe; we defer the reader to the development in [13].
and summarize a key point below.

Figure 2.2: An example of current-mode control

A major feature of current-mode control is that even with no extra compensation ($H(s) = 1$), the characteristic equation is reduced to first-order through the elimination of the inductor branch characteristic, which implies a less onerous transfer function shaping task for the system designer. This model reduction is achieved by the minor feedback loop, which converts the inductor into a controlled current source. However, the current control mechanism is only easily conceptualized in the time-domain. This makes it difficult to discuss current-mode controllers using systematic, control-theoretic techniques. In particular, a well-known phenomenon termed subharmonic oscillations occurs under simple current-mode control when the duty cycle is above 0.5 [13]. While this behavior and techniques for suppressing it are well-understood, it is not straightforward to predict its occurrence using LTI models.

**Restrictions**

The primary restrictions of any linear control scheme are rooted in the achievable dynamics of linear systems: in response to step perturbations at any terminal of interest, the settling behavior
must be exponentially damped (with or without oscillations), and only asymptotically reaches the steady-state value. While the asymptotic reaching presents little practical obstacle to realizing the desired steady-state converter behavior, it poses limits in how quickly the system may ever be expected to settle. At a switching frequency of 50 MHz, conservative design might place the unity gain frequency one decade lower at 5 MHz, yielding a characteristic time constant of 200 ns. Several time constants are needed for the regulator system to settle, precluding the use of such a regulator for aggressively temporally granular DVFS schemes.

Additionally, all averaging techniques must discard information about the dynamics of the true system, and so the designer must always understand that the design procedures carried out are targeting a severely approximated version of the true system. The LTI system under analysis no longer contains information about the switching dynamics of the true system, and so there remains limits to the trustworthiness of the design equations. However, it must be repeated that these indiscretions with the system analysis allow for significantly more powerful design techniques to be used, and the design techniques remain valid so long as an appropriate margin is kept between the relevant frequencies of the linear dynamics and the switching frequency. Ultimately, the controller design always needs to be vetted in hardware.

As a warning about averaging techniques, subharmonic oscillations in current-mode control are not universally predicted in all time-averaged models. The root cause for this disagreement between models is that in current-mode control, the duty cycle of the switching signal is controlled in an indirect way, and so averaging these systems requires establishing an appropriate average mathematical relationship between the duty cycle and the state variables. Numerous such relationships have been suggested in the literature, and yield quite different insights into the dynamic performance of the system, with many unable to predict the instability above 50% duty cycle [73].
2.3 Variable-Structure Systems

A formalism around variable-structure systems was developed starting in the 1950s as a way to understand systems that involved relays as high-speed switching elements, especially as a potential replacement for analogue electronic control. Rather than using averaging techniques, as the circuit design community did when faced with a similar class of systems, variable-structure control theorists sought to maximally understand the system without approximating the system beyond idealizing some strictly parasitic dynamics. We shall see that this take on the system analysis leads to a fundamentally different insight than that provided by the PWM, fixed-frequency picture provided above.

Variable-structure system analysis also developed concurrently with the formalization of so-called optimal control theory, a branch of control theory that seeks to optimize state trajectories according to some metric. It is a well-known result that given bounded control constraints, time-optimal trajectories involve some sort of bang-bang behavior that may settle to some sort of singular trajectory [80]; the simplicity of implementing such a control scheme (sans singular trajectory) using relays or switches is a pleasant bonus.

Variable-structure methods have been used successfully to understand control systems across a multitude of different fields: mechanical systems [81], chemical plants [82], economic systems [83], etc. It is a source of mild consternation to the author that the circuit design community has effectively ignored the existing literature from the broader control theory community and created their own vocabulary and conceptual understanding that ends up being painfully limited to power converters. This informs the re-casting of buck converter control as a variable-structure problem in the remainder of this chapter. Though such a viewpoint is not new [5], this work seeks to bring it further into the mainstream, so as to hasten the adoption of this powerful analysis framework in integrated converter design.
**Sliding-Mode Control**

Sliding-mode control is a paradigm for design of variable-structure control system design that revolves around the construction of a sliding surface $\sigma(t) = 0$ in the state space of the system onto which the system is driven \[84\]. The function $\sigma(t)$ is chosen to be a single-valued function of the system states and is involved in the construction of an appropriate control law. In particular, first-order sliding mode control theory considers systems whose feedback involves the signum function acting on $\sigma(t)$. The design of comparator-modulated buck converters has been previously explored in the sliding mode context, resulting in effective new architectures for buck converter control \[85\].

Sliding-mode control may be viewed as a design paradigm within the larger framework of variable-structure system theory, and articulates a ‘how’ to defining the structures of interest, constraining the switching behavior between them, and shaping those to achieve the desired transient and steady-state behavior. In particular, focus is put on the desired state trajectory, and how to articulate a control law based on the system states to actuate the switches. There are a host of different types of control within sliding-mode control, distinguished by the specific nature of the feedback used to generate the control law for switching \[86\]. Here, we will only consider classical first-order sliding-mode control (classical 1-SMC), which limits the control law to acting on some combination of the signs of the states.

Major features of well-implemented sliding-mode control are robustness to parametric uncertainty, simplicity of implementation, finite-time reaching of a desired steady-state, and system order reduction through specification of a sliding surface where higher order dynamics are never excited. However, these features are lost when uncertainty in dynamics (as opposed to in system parameters) is present: unmodeled parasitic dynamics will result in an inability to converge exactly to $\sigma(t) = 0$. 
**Chattering**

In all practical systems, parasitic dynamics such as delay from control to relay output will cause deviations of the state trajectory from the prescribed surface. Rather, the states will oscillate in a neighborhood of $\sigma(t) = 0$ defined by the characteristics of the parasitic dynamics. This oscillatory behavior is termed *chattering*. In the mechanical context, the oscillatory nature of chattering causes wear and tear on moving parts. In the electrical context, chattering results in consumption of energy in switching switch states. As a result, much of the development of sliding-mode control has been in devising techniques to suppress chattering, with much effort being put towards use of more complex control laws that act on, e.g., signs of derivatives of states \[87\].

### 2.4 The Bang-Bang Buck Control Family

With the growing awareness of bang-bang control, it was inevitable that engineers would apply those techniques to power converters as well, especially given that DC-DC converters were already well-understood as switching systems. In this section, we consider some historical and theoretical trends that lead to the specific converter topologies to be analyzed in the latter portion of this chapter.

**Ripple-Based Switching**

The discussion of linear control assumed that the switching signals are being generated independently with absolute control. Investigation of practical generation and limitations of existing systems have been discussed exhaustively in other references \[88\]. However, to pave fundamental ideas for the sliding-mode control techniques that are the focus of this section, we first discuss
the idea of switching signal generation through signals wholly internal to the basic switched-inductor converter.

Through a non-linear operator such as a signum/relay with or without hysteresis (implemented by, e.g., a comparator), a signal with content at non-zero frequencies may be transformed into a two-level signal, as would be suitable for use in controlling MOSFET switches. Within the buck converter, there are several signals that require content at non-zero frequencies during steady-state operation: the inductor current, the output voltage, and the switching node. Ignoring the question of start-up, we may add a relay block acting on one or more of the non-DC signals and feed its two-level output back as the switch control signal. Correctly constructed, steady-state oscillations should be sustainable.

The above description is left intentionally vague so as not to over-constrain the underlying idea of treating the system as an undriven oscillator. The design questions are then of course quite varied:

- How may be the oscillations be controlled to yield the desired output voltage?
- Which signal is the 'optimal' one for generation of the switching signals?
- How may start-up be guaranteed?

Of primary interest is the implementation detailed [89], which describes the circuit as a 'hysteretic PWM' converter. The ripple that generates the PWM signal is taken from the inductor current, and is transformed into a two-level signal using a hysteretic comparator. We can immediately see that in the absence of time delay through the comparator and hysteresis in the comparator, the two-level signal should have arbitrarily high frequency – this is the manifestation of chattering in this system. From that, it is similarly easy to understand that this simple hysteretic or bang-bang controller scheme for buck converters is understood can have very fast transient
response due to its non-linear dynamics, but has the potential drawback that the switching frequencies are heavily load-dependent.

An additional complication particularly cogent to the analysis in this work is that when operating with thin-film inductors, non-fixed switching frequency could result in highly variable efficiencies during operation due to the process-dependent AC loss mechanisms detailed in section 1.1. In order to have any sort of predictability of designs that use these inductors, a fixed switching frequency scheme is necessary.

**Consequences of Chattering**

Chattering in these systems is no longer to be exclusively demonized: once we consider internally-generated-ripple-controlled systems as variable-structure systems to be viewed through the lens of chattering, we can see that chattering itself is responsible for generating the ripple that we depend on to generate the switching signals in the first place – and indeed, once we have bitten the hard-switching converter bullet (cf. section 1.1), we must have chattering within the system. However, the primary negative manifestation of chattering in a classic 1-SMC controller is as a switching frequency that is highly sensitive to circuit variation and operating conditions [84].

In the context of a larger system, this implies an increase in complexity of electromagnetic interference (EMI) mitigation schemes, and similarly, an increase in complexity of ripple reduction filters both upstream and downstream of the DC-DC voltage converter itself. With single-frequency operation, as might be found in a controller using simple LTI techniques, such filters are often realized as simple notch filters [13]. However, if the frequency is known to vary, and if the frequency range itself also varies with circuit variation, then a more complex bandpass filter is necessary.
2.5 Asymptotic Stability of One Class of Bang-Bang Controller

In this section, we consider the Lyapunov stability of the bang-bang controller topology of figure 2.3a which uses inductor current sample to generate the control ripple. For simplicity, the half-bridge is absorbed into the inverting comparator. Figure 2.3b depicts the linear, third-order portion of the system, to which a bang-bang or relay control law $V_x(t)$ is applied at the indicated note. We assume that the control law is actuated instantaneously in this section, and will consider the treatment of chattering separately. We will use R and G implicitly for components that obey Ohm’s law to represent the resistance and conductance.

Definition of Terms

We are primarily concerned with broad notions of stability in non-linear dynamical systems. We follow the development of Lyapunov as detailed in [71].

Lyapunov stability: consider a particular vector trajectory $x_0(t)$ with prescribed initial condition $x_0(a)$. The trajectory $x_0(t)$ is stable if for all $\epsilon > 0$, $\exists \delta > 0$ such that if $\|x(a) - x_0(a)\| < \delta$, $\|x(t) - x_0(t)\| < \epsilon \forall t \geq a$.

Lyapunov asymptotic stability: given the definitions above, if $x_0$ is stable and $\lim_{t \to \infty} \|x(t) - x_0(t)\| = 0$, then $x_0(t)$ is asymptotically stable.

We will hereafter refer to Lyapunov stability and asymptotic stability as just ‘stability’ and ‘asymptotic stability’. A trajectory is stable if we can always choose initial conditions that generate a second trajectory that stay within a well-defined neighborhood of the stable trajectory. It is asymptotically stable if that neighborhood becomes arbitrarily small with increasing time.

These definitions are relevant for understanding the bang-bang controller as asymptotic stability of a desired steady-state trajectory implies that the system will be able to reject disturbances. Though the strict definition of asymptotic stability does not prescribe a time within
(a) An ideal bang-bang controller using inductor current sampling

(b) The linear portion of the system

(c) The full system, with non-zero parasitic resistance

Figure 2.3: Circuits for the bang-bang controller
which the effects of the disturbance are eliminated, we shall see that it is possible to determine bounds on the time.

We further define important concepts that are used in the so-called ‘direct method of Lyapunov’ to demonstrate stability of a trajectory.

**Positive definite functions**: consider a single-valued function $V(x)$ defined in a neighborhood $R$ of the origin. If 1) $V(x)$ is continuously differentiable in $R$, 2) $V(0) = 0$, and 3) $V(x) > 0$ when $x \in R \setminus 0$, then $V(x)$ is positive definite (PD) in $R$.

**Positive definite functions of time**: consider a single-valued function $V(t,x)$ defined in a neighborhood $R$ of the origin. If 1) $V(x)$ is continuously differentiable in $R$ for $t \geq a$, 2) $V(t,0) = 0 \forall t \geq a$, and 3) $V(t,x) \geq$ some PD $W(x)$ when $x \in R, t \geq a$ then $V(t,x)$ is PD in $R$.

**Lyapunov functions**: consider a neighborhood $R$ of $x = 0$, and some $V(t,x)$ PD in $R$. $V$ is a Lyapunov function for some system $\dot{x} = f(t,x)$ if $\dot{V} \leq 0 \forall x \in R, t \geq a$. The dot operator here is a non-standard derivative operator, and denotes the sum of the partial derivatives with respect to time and each of the dimensions of the space of interest. We will abuse the notation slightly: where the dot operator is used in the context of Lyapunov functions, it will define this special operation. Otherwise, we will use it to denote the time derivative operation.

If a Lyapunov function in $R$ exists for the system of interest, then the origin of the space is stable. Moreover, if $-\dot{V}$ is PD in $R$, and $V(t,x) \leq W(x)$ for some $W(x)$ PD in $R$, then the origin is asymptotically stable. This is the crux upon which Lyapunov’s direct method lies upon. Proof and further explanation may be found in [71].
Stability Proof

As state variables for this system, choose:

\[ x_1 = V_{\text{out}} - V_{\text{ref}} \quad (2.5.1) \]
\[ x_2 = V_{\text{cfb}} \quad (2.5.2) \]
\[ x_3 = i_L - V_{\text{ref}} G_{\text{load}} \quad (2.5.3) \]
\[ x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}^T \quad (2.5.4) \]

For brevity, the time dependence of the node voltages is left implied. With this selection of state variables, the following control law acts to bring the state vector to zero:

\[ V_x(t) = \frac{V_{\text{in}}}{2} (\text{sgn} \sigma + 1) \quad (2.5.5) \]
\[ \sigma \equiv -x_1 - x_2 = V_{\text{ref}} - V_{\text{out}} - V_{\text{cfb}} \quad (2.5.6) \]

Here, \( \sigma \) represents the particular constant sliding surface involved with this control architecture. Here as well, the time-dependence of \( \sigma \) is left implied.

To demonstrate the asymptotic Lyapunov stability of this system, we choose the following positive definite function of \( \sigma \) as a candidate Lyapunov function, based on classical sliding mode control [84]:

\[ V(t, x) = \sigma^2 / 2 \quad (2.5.7) \]

\( V(t, x) \) is noted to be positive definite. If the condition on the time derivative \( \dot{V} = \dot{\sigma} \sigma < 0 \) holds for all \( x \in \mathbb{R}, \ t \geq t_f \), then \( V(t, x) \) is a Lyapunov function and the system is asymptotically stable for \( t \geq t_f \), since the system always acts to move the state vector towards the zero state.

For \( \dot{\sigma} < 0 \), \( \dot{\sigma} = -\dot{x}_1 - \dot{x}_2 = (V_{\text{in}} - V_{\text{out}} - V_{\text{cfb}}) / (R_{\text{fb}} C) + (V_{\text{in}} - V_{\text{out}} - V_{\text{cfb}}) / (R_{\text{fb}} C_{\text{fb}}) \), which is pos-
itive for $V_{in} - V_{out} - V_{cfb} > 0$.

For $\dot{\sigma} > 0$, $\dot{\sigma} = (V_{out} - V_{cfb}) / (R_{fb} C) + (-V_{out} - V_{cfb}) / (R_{fb} C_{fb})$, which is negative for $-V_{out} - V_{cfb} < 0$.

Under these assumptions, which are valid for the general operation of the buck converter, $\dot{V}$ is negative and $V(t, x)$ is a valid Lyapunov function, such that the system is asymptotically stable.

In the presence of a parasitic equivalent series resistance $R_L$ (figure 2.3c), it suffices to redefine the states as:

\[ x_1 = V_{out} - V_{ref} - R_L i_L \]  
(2.5.8)

\[ x_2 = V_{cfb} - R_L i_L \]  
(2.5.9)

\[ x_3 = i_L - (V_{ref} - R_L i_L) G_{load} \]  
(2.5.10)

The control law and Lyapunov function with respect to the states are unchanged and act to move the states towards the zero state; the modifications here include the systematic droop due to the presence of the series resistance.

### 2.6 Injection Locking for Fixed Switching Frequency Behavior

The above development assumes that $V_x$ responds instantaneously to changes in $V_{out}$ and $V_{cfb}$.

As discussed in section 2.4, in the presence of parasitic, unmodeled dynamics such as those arising from the finite bandwidth of a physical realization of a comparator, the phenomenon of chattering occurs. Eliminating chattering alone would come at the cost of efficiency, since it would imply that the half-bridge is no longer being hard-switched. Because our objective in designing these switched-inductor regulators is not to eliminate the chattering, but rather to control its frequency exactly, we now consider modifications of the underlying system that achieve said
In this section, we discuss injection locking through modulation of the control input and its analysis within the sliding mode framework. A time-domain analysis of the response of the system is also performed that corroborates the locking mechanism. Theoretical limits on the locking range are discussed; the non-infinite lock-in range of this scheme has the additional benefit that the transient response is not limited by the desired steady-state switching frequency.

Injection locking [90], a well-known phenomenon that broadly describes any tendency for a non-linear oscillator’s center frequency to be affected by external sources that couple into the oscillator system. Within the framework of sliding mode control, the chattering is a manifestation of a free-running non-linear oscillator embedded in the system. Previous work has exploited the free-running oscillator nature of the core bang-bang control scheme to achieve frequency control [40] [91] [92] but has not discussed full implementation details nor considered what requirements on steady-state lock stability imply for component selection. The latter concern is especially important for the fully integrated context, where access to high quality resistors and capacitors over a wide spread of component values is not available.

Introduction of hysteresis is the framework most commonly associated with chattering frequency control in this class of non-linear buck converter controllers [85]. Alternatively, dwell-time-based control through introduction of a delay in the loop has also been investigated in these systems [93]. Both techniques result in identical system behavior in the buck converter and may be analyzed through their impact on limit cycling behavior in the system. If we restrict the discussion to a hysteresis-enabled frequency control, then a frequency domain analysis using a describing function for the hysteretic comparator may be carried out, predicting the existence of a finite-valued frequency harmonic balance [94]. The frequency for which this balance exists depends on the linear transfer function from the control node $V_x$ to the comparator, as well
as the rail voltages of the comparator. This succinctly corroborates the well-known result that
the oscillation frequency of hysteretic-comparator-controlled buck converters is a function of
the line voltage, transmitted through the describing function of the comparator, and of the load
voltage, through the transfer function of the linear portion of the controller [89]. Thus, control-
ling the chattering/limit cycle frequency to a single value independent of load or line conditions
is not possible without introduction of additional feedback mechanisms to adjust the hysteresis
band/delay time dynamically.

**Theoretical Details**

To implement injection locking in this system, we identify that the switching surface depends
on the value of $V_{\text{ref}}$ and note that controlling $V_{\text{ref}}$ as a function of time is equivalent to open-loop
time-domain modulation of the switching surface $\sigma$ itself. If the chattering frequency of the
system is kept below the modulation frequency of $\sigma$, it has been previously determined that the
switching frequency may be bounded [93]. In this work, we demonstrate a simple augmentation
to the system that allows it to track exactly the switching surface at the prescribed frequency
while suppressing the natural chattering.

Chattering may be characterized more rigorously as a manifestation of unstable dynamics
in a neighborhood of the sliding surface [84], with the specific size of the neighborhood a de-
tailed function of the system. Outside of this neighborhood, the desired trajectory appears to be
Lyapunov stable, but within the neighborhood, the constructed control law no longer drives the
state trajectory onto the sliding surface. The rationale behind modulation of the switching sur-
face to suppress chattering is motivated by the observation that if the state trajectory is kept out
of the unstable neighborhood, then chattering (in the narrow sense) should never be observed,
as the dynamics responsible for chattering are do not contribute to the state trajectory. The use
of a time-varying switching surface has been explored to design desired dynamics in power converters. Here, we use it to define the switching frequency exactly, which is especially important given the earlier analysis of the impact of switching frequency on efficiency.

The new target switching surface $\tilde{\sigma}$ with an unstable neighborhood (denoted region II) due to the comparator dynamics is indicated on figure 2.4 using $\sigma$ as the vertical axis. If the sliding variable is in regions I or III, the system drives the sliding variable towards region II. Within region II, the sliding variable is not moved unconditionally towards $\tilde{\sigma}(t)$, but travels through towards regions I or III, depending on the previous system trajectory. In the case where $\tilde{\sigma}(t) = 0$, $\sigma(t)$ would then be confined to region II and chattering would occur. However, we choose here a non-constant $\tilde{\sigma}(t)$ shaped such that the sliding variable will always exit the unstable region II and be forced to track the non-constant $\tilde{\sigma}(t)$ at the prescribed frequency.

![Figure 2.4: A target switching trajectory with an unstable neighborhood](image)

In this new system, $\sigma(t) = 0$ continues to represent the desired system performance, as opposed to $\tilde{\sigma}(t) = 0$. The action of the control law stabilizes the switching frequency, but at the cost of giving rise to a $\sigma(t)$ trajectory whose steady-steady behavior does not lie in the desired neighborhood of $\sigma(t) = 0$. Consider the example of figure 2.5 where the average value of $\sigma(t)$ is not close to zero, even though that of $\tilde{\sigma}(t)$ is. Indeed, the average value can lie within the whole range spanned by $V_{\text{ref}}(t)$, with a strong dependence on the slope of the feedback signal and the
duty cycle of the square wave used to generate $V_{\text{ref}}(t)$ \[5\]. As a result, the output voltage of the converter would be seen to deviate from the desired reference voltage.

![Diagram of a square wave with duty cycle and time axis](image)

Figure 2.5: A potential, undesired trajectory if a varying switching surface alone is used, from \[5\]

An additional source of output voltage error is introduced by the DC resistance of the inductance, which degrades the load-line resistance performance directly, and is unavoidable in the bang-bang controller as presented thus far \[89\]. With thin-film inductors, which may display significant DC resistance, the corresponding voltage droop becomes an even larger issue.

A quasi-$V^2$ control architecture \[96\] corrects for voltage droop in the output system by introducing a voltage-mode feedback loop around the entire system to minimize the steady-state error between the output voltage and the target reference voltage. In this system, the average value of the PWM signal is compared with the average value of the feedback voltage (the regulated output voltage), and the error is used to adjust the duty cycle of the PWM signal in the outer feedback loop, which impacts both the slope and the average value of $V_{\text{ref}}(t)$. Properly implemented, the duty cycle of the injection signal will settle to a value consistent with forcing a state trajectory close to $\sigma(t) = 0$. 
Implementation Details

Figure 2.6 depicts details of a candidate frequency control scheme in steady state. An square wave of period T, switching from 0 to $V_H$, is filtered and then driven onto the positive terminal of the comparator. The square wave is generated digitally using a standard digital pulse width modulation (DPWM) block. For the purposes of this analysis, we assume the duty cycle $D$ to be constant and known such that the average value of the RC-filtered square wave over an integer number of periods of the square wave is $D V_{in}$. Assuming that the input capacitance of the comparator is negligible, the RC filtered waveform over one period from 0 to T is:

\[ v_1(t) = v_0 + \left( 1 - e^{\frac{-t}{R_{inj}C_{inj}}} \right) (V_H - v_0) \quad \text{for } 0 \leq t \leq DT \quad (2.6.1a) \]

\[ v_1(t) = \left[ v_0 + \left( 1 - e^{\frac{-DT}{R_{inj}C_{inj}}} \right) (V_H - v_0) \right] e^{\frac{-(t-DT)}{R_{inj}C_{inj}}} \quad \text{for } DT \leq t \leq T \quad (2.6.1b) \]

$v_0$ is the initial voltage during one such period of steady-state operation such that $v_1(0) = v_2(T) = v_0$, and may be expressed as:

\[ v_0 = V_H \frac{1 - e^{\frac{-DT}{R_{inj}C_{inj}}}}{e^{\frac{-(1-DT)}{R_{inj}C_{inj}}} - e^{\frac{-DT}{R_{inj}C_{inj}}}} \quad (2.6.2) \]

Note that the above quantity is strictly less than $V_H$. If we make the assumption that $V_{out}$ remains constant (the classical small-ripple approximation \[13\]), the forms of the waveform are
exactly those of equation family (2.6.1), except they are governed by $R_{fb}$ and $C_{fb}$, instead.

In order to maintain frequency synchronization, $v_1(t)$ must be kept greater than $v_{f1}(t)$, and $v_2(t)$ must be kept below $v_{f2}(t)$ such that the characteristics of the RC-filtered square wave completely define the comparator output frequency.

The outer feedback loop is implemented in an analogue fashion: a delayed version of the base DPWM signal is logically OR’d with the base signal itself, and the delay is controlled by the output of the error amplifier. In this way, limit cycles that may arise due to the duty cycle quantization inherent to DPWM blocks [88] are eliminated while retaining the implementation simplicity of the DPWM square wave generator and enabling the outer voltage loop in a conceptually simple manner. A step load current change affects this control system by forcing $\sigma(t)$ away from the switching surface (into regions I or III of figure 2.4) due to the change in $V_{out}$. At this point, the system is no longer in an injection-locked state such that the frequency is no longer fixed, but will act to drive the sliding variable back towards region II optimally. Once within region II, the injection locking mechanism within this non-linear system should reassert fixed-frequency behavior.

The detailed behavior of the locking transient and a rigorous stability analysis of the full quasi-$V^2$ controller is non-straightforward due to the multiple non-linear interactions between the slopes of the injection signal and the feedback signal and the duty cycle control signal. Simulations of an idealized system and hardware verification were carried out to validate the behavior of the system; the stability of the system is discussed in section 3.4.
The previous two chapters concerned themselves primarily with laying theoretical frameworks of interest to bang-bang controllers using thin-film inductors. While we have demonstrated the theoretical asymptotic stability of the controller, we still need to demonstrate that a practical deployment will respond in a manner that fulfills the specifications on transient performance of the converter. Moreover, the start-up and stability of the injection-locked bang-bang augmentation were not analyzed in depth. In this chapter, we will present detailed results that corroborate the theoretical claims made previously.
3.1 Introduction to 3D Interposers

Because interposers are used in these demonstrations, we go into some more detail on interposer technologies here. A silicon interposer is a wafer/die with vias that penetrate from the top side to the back, or grind side of the wafer. These vias are termed through-silicon vias (TSVs) for clear reasons. Construction of these vias typically involves a deep anisotropic etch from the top side into the substrate to a depth of approximately 100 µm, filling in of the resulting trench then thinning from the grind side to free the vias\textsuperscript{97, 98}. As a result, interposer thickness is determined by the achievable aspect ratios of that first top-side etch/fill. This step is usually performed after the front-end processing is complete but before the back-end build-up starts, making this a \textit{via-middle} process\textsuperscript{99}.

Active interposer technology, where front-end devices co-exist with TSVs, has recently come to the fore of bleeding-edge packaging technologies as a costly but high-performance solution to communication bandwidth problems in large systems\textsuperscript{100}. Perhaps the best known examples are memory cubes\textsuperscript{101}, which use TSV-enabled DRAM dies in a vertical stack to increase areal density and bandwidth. Owing to the regularity of the DRAM designs, yield optimization for these designs is tractable. However, for generic applications, interposers remain a niche packaging technique owing to the difficulty of maintaining acceptable cost and high yield. Chip-on-wafer-on-substrate\textsuperscript{102} or integrated fan-out\textsuperscript{103} technologies have emerged to bridge the performance gap at an acceptable cost, and have quickly spread in the space despite their later development.
3.2 Testing Module Construction

The front-end design was overseen by Noah Sturcken during his time in the Bioelectronic Systems Lab. The substrate fabrication was overseen by Kevin Tien. Assembly of the modules was carried out by collaborators at IBM Research and Ferric Inc.

Front-End Design

A schematic of the regulator front-end circuitry [59] is provided in figure 3.1. This front-end is designed and fabricated in the now-defunct IBM 32 nm silicon-on-insulator process, and is a relatively aggressively scaled technology to use in this space. However, the improved core switches in this technology suggest that a system designed around this technology may be able to switch fast enough to suppress hysteretic losses while maintaining sufficiently low dynamic loss in the switches.

The back-end input-output (I/O) interface finish is 3-on-8 C4 area array to maximize the number of interconnections to the front-end. The interconnection from the front-end circuitry to the off-chip inductors was performed by routing in a top redistribution layer to a dedicated I/O area. The I/O image with inductor connections indicated is depicted in figure 3.2.

Inductor Design

Access was provided to two types of inductors: solenoidal, open-core inductors as IPDs through Ferric Inc. [52], and magnetic-clad yoke inductors as passive interposer through IBM Research [104]. Only one topology for each was selected for demonstration, and salient technology and realization features are provided in table 3.1. M-H curves are provided here for the interposer-deployed technology in figure 3.3.
Figure 3.1: Schematic of converter circuitry, from [59]

Figure 3.2: Layout image of IO pattern for silicon die
Table 3.1: Inductor technology summary

<table>
<thead>
<tr>
<th></th>
<th>Interposer</th>
<th>IPD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic material</td>
<td>Ni$<em>{45}$Fe$</em>{55}$</td>
<td>Amorphous cobalt alloy</td>
</tr>
<tr>
<td>Coercivity</td>
<td>&lt; 1 Oe</td>
<td>&lt; 1 Oe</td>
</tr>
<tr>
<td>DC Saturation Field</td>
<td>25 Oe</td>
<td>15 Oe</td>
</tr>
<tr>
<td>Core/cladding lamination?</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Magnetic layer deposition</td>
<td>Electroplated</td>
<td>Undisclosed</td>
</tr>
<tr>
<td>Magnetic layer thickness</td>
<td>1 µm</td>
<td>Undisclosed</td>
</tr>
<tr>
<td>Conductor (Cu) thickness</td>
<td>5 µm</td>
<td>Undisclosed</td>
</tr>
</tbody>
</table>

Figure 3.3: Representative M-H curves for the magnetic material used on the interposer. The red curve is the hard axis, and the blue curve the easy axis.

**Substrate Design**

Owing to the aggressiveness of the C4 pitch, the substrate design necessitated the use of build-up substrate technologies [105] that were previously not well-understood in the Bioelectronic Systems Lab. An initial design where the vendor was unable to meet solder mask specifications and left parts of the chip-attach area non-solder mask defined (non-SMD) ultimately was deemed incompatible with certain parts of the interposer assembly flow, and a re-spin of the substrate package was performed. Ultimately, two substrates nearly identical in design, but fabricated by two different vendors were used in the demonstrations to be discussed in the latter half of this chapter.
Assembly

Assembly of the IPD-based modules was performed in-house with significant assistance from Ryan Davies (Ferric Inc.) using a Finetech FINEPLACER lambda (figure 3.4) to perform the requisite flip-chip attachment of the chip. The FINEPLACER lambda is capable (nominally) of single-micron precision and of bonding while controlling pressure and applying heat to both substrate and flip-chip component. The IPDs were provided with a tin eutectic-capped copper pillar finish, distinct from the high-temperature lead-less C4 finish on the chip. The IPDs were assembled using a lower-temperature manual hot air reflow step. A diagram of the module is presented as figure 3.6.

The interposer module was assembled by IBM Research collaborators (Bing Dang, Paul Andry, Jae-woong Nah et al.) in a significantly more complex manner. Owing to the low thickness of the interposer (approx. 100 µm), it is not possible to handle it directly, and it must be bonded to a handle wafer to provide stability. During thinning, the grind side of the passive interposer wafer is bonded strongly to a glass handle wafer. The active die is then first bonded onto the interposer using standard flip-chip techniques, then released from the handle wafer using excimer laser ablation at the interface. The released interposer surface is cleaned, and then bonded to the substrate using injection-molded soldering techniques [106], as the grind side of the interposer was left unbumped. A diagram of the module is presented as figure 3.5.

The TSVs themselves are fabricated in a TiN/W, insulated-via process that is known to be CMOS-compatible [107].

Pictures of completed modules are provided as figure 3.7. SEM cross-sections depicting the full chip-interposer-substrate stack-up are provided in figure 3.8. The interposer layout is depicted in figure 3.9; the visible green circles are TSVs, and the hollow circles are the face-to-face-only attachment from the inductors to the regulator.
Figure 3.4: The Finetech FINEPLACER lambda

Figure 3.5: Illustration of the interposer-based module stack
An important note on the interposer module assembly: the yield was exceedingly low, even by academic standards, and required management across a large team to complete. Thus, our experience is that use of the interposer demands trading away a significant amount of time, effort, and money for what at the module level may not be a particularly useful gain.

### 3.3 Board-Level Testbench

Testing, including incremental board design and assembly, was performed by Kevin Tien and Fengqi Zhang.

The testing motherboard supplies all off-chip power nets of interest through linear regulators. Analogue data from on-board current and voltage sensing points are digitized using a bank of multi-channel ADCs, and an Opal Kelly XEM3010 is used to instrument the testing, including programming the chip configuration registers and reading in the streaming digitized data.
(a) Interposer-based module, close-up on attachment area

(b) IPD-based module, with more details on the substrate layout

Figure 3.7
Figure 3.8: Sequential close-ups of the interposer module stack-up, originals courtesy of Jae-woong Nah
from the ADC banks. A MATLAB interface to the Opal Kelly is used for data visualization and post-processing. The board includes off-chip current loads for static testing.

Pictures of two generations of testing board are provided in figure 3.10

### 3.4 Experimental Results

The experimental results presented in this work focus on corroborating the insights of the first two chapters. Moreover, because of the aforementioned yield issues with the interposer module, there are more in-depth results available for the IPD-based module.
(a) First-generation testing board

(b) Third-generation testing board, courtesy of Fengqi Zhang

Figure 3.10
Interposer-Deployed Yoke Inductor System

First, we present the traditional efficiency vs. output current plot for the converter running with all eight-phases on at a fixed conversion of 1.66 V to 0.83 V in figure 3.11. Within each curve, we expect the efficiency to increase from 0, as the output power increases, and then reach a plateau with negative slope, as conduction losses increase. We note that there is indeed an efficiency peak with respect to frequency, indicating that AC losses in the inductor dominate below 150 MHz, but are suppressed enough such that dynamic losses in the switches dominate significantly at higher frequencies.

In figure 3.12, we present curves for efficiency at various operating frequencies, changing only $V_{in}$ and keeping the duty cycle constant. Because these changes are not expected to change the THD of the inductor current, but do change the fundamental frequency amplitude, we expect the AC losses to go down continually. However, because the power delivered is also decreasing, the efficiency should go down with decreasing output voltage as well. Interestingly, we note that at low conversion ratios, operating at 175 MHz offers a significant efficiency improvement. This may be attributed to the extremely low fundamental amplitude in that operating regime, as $V_{in}$ affects the fundamental amplitude directly (cf. equation (1.2.8)). As $V_{in}$ increases, the fundamental amplitude increases, and the correspondingly higher core loss at 175 MHz vs. 150 or 125 MHz acts to cause the efficiency to saturate.

We also present a transient response to a large-step start-up as an example of a stable ramp-up to a steady-state in figure 3.13. The response is clearly segmented into two parts: the initial approach is due to the reaching phase of the bang-bang control, and as the sliding surface is reached and the injection pulling begins, the outer voltage loop takes over and a linear (that is, asymptotic) settling phase begins.

A peak efficiency of 82% for conversion from 1.66 V to 0.83 V is observed over eight-phase
operation at a 150 MHz per-phase switching frequency. The use of multiple phases, pair-wise negatively coupled, is essential to mitigating the loss mechanisms in this inductor technology that would otherwise cause globally high efficiency losses, as outlined in section 1.1.

Figure 3.11: Efficiency vs. load current at varying $V_{\text{in}}$, interposer module

Figure 3.12: Efficiency vs. input voltage with fixed load current, interposer module
Efficiencies plotted as a function of load current for the IPD-deployed system are unsurprising and yield no extra insight. We instead present augmented graphs that look directly at behavior versus duty cycle at various load currents; the effect of load current on efficiency may be gleaned readily from these data. Efficiencies at 75 MHz and 125 MHz per-phase switching frequency at varying load currents are presented in figure 3.15. Here, duty cycle is a proxy for conversion ratio; graphs indicating representative data relating duty cycle to conversion ratio are provided in figure 3.14.

We may see in figure 3.15 that there is a distinct flattening-out of the efficiency curves around 50% duty cycle at low load. At higher loads, the effect is less pronounced, and at lower frequencies the effect is slightly more pronounced. With a representative Verilog-A model (courtesy of Ferric Inc.) for an inductor in this technology, simulation results (figure 3.16) in an otherwise ideal single-phase converter corroborate this behavior at low switching frequency, which we find quite notable and will discuss further in section 3.4.

Efficiency as a function of switching frequency is presented in figure 3.17, at fixed duty cycle and current. As discussed in section 1.1, the marked increase in efficiency as a function of
switching frequency is not in line with traditional wisdom around buck converters, and arises completely from the increase in frequency-dependent core losses in these types of converters. As switching frequency increases, both THD and the magnitude of the fundamental drop, and at around 80 MHz, they are low enough such that the ideal inductor assumption is more accurate and the efficiency begins dropping off slowly due to the continued increase in dynamic losses.

**Potential Non-Monotonicity in Efficiency vs. Duty Cycle**

Consider the following formulation of efficiency based on the power delivered to the load as a function of duty cycle $P_{out}(D)$, the power lost in the converter as a function of duty cycle $P_{loss}(D)$, and the derivative thereof:
Figure 3.15: Efficiency vs. duty cycle, IPD-based module

(a) 75 MHz per-phase switching frequency

(b) 125 MHz per-phase switching frequency
Figure 3.16: Efficiency vs. duty cycle, simulated with Ferric Inc. physics-based thin-film inductor model, 15 MHz switching frequency

Figure 3.17: Efficiency vs. frequency, IPD-based module

\[
\eta(D) = \frac{P_{\text{out}}(D)}{P_{\text{out}}(D) + P_{\text{loss}}(D)} = \frac{I_{\text{out}}DV_{\text{in}}}{I_{\text{out}}DV_{\text{in}} + P_{\text{loss}}(D)} \tag{3.4.1}
\]

\[
\frac{d\eta}{dD} = \frac{I_{\text{out}}DV_{\text{in}}(I_{\text{out}}DV_{\text{in}} + P_{\text{loss}}(D)) - I_{\text{out}}DV_{\text{in}} \left( I_{\text{out}}DV_{\text{in}} + \frac{dP_{\text{loss}}}{dD} \right)}{(I_{\text{out}}DV_{\text{in}} + P_{\text{loss}}(D))^2} \tag{3.4.2}
\]

\[
= \frac{I_{\text{out}}DV_{\text{in}} \left( P_{\text{loss}}(D) - D \frac{dP_{\text{loss}}}{dD} \right)}{(I_{\text{out}}DV_{\text{in}} + P_{\text{loss}}(D))^2} \tag{3.4.3}
\]

From the above, it is immediately clear that is it theoretically possible for efficiency behavior to be even non-monotonic with respect to duty cycle, and that the exact behavior is a strong
function of the relationship between power loss and duty cycle. Because the fundamental amplitude is globally maximum at a duty cycle of 50% and the THD is globally minimum at that same duty cycle, we expect $\frac{dP_{loss}}{dD}$ to have the largest impact at 50% duty cycle, an expectation corroborated by the experimental results of the IPD-based converter deployment.

The discrepancies between the frequencies where the effect is observed in the model vs. in experimental results is yet unexplained. We suspect that either the over-idealization of the simulation testbench leads to more power delivered to the load, skewing the efficiency measurements. Additionally, further investigation needs to be made into process variability in the inductor technology to confirm that the model is indeed an accurate representation of the inductor behavior.
Conclusion

This thesis is meant as a detailed exploration of heterogeneous integration of thin-film magnetic inductors in fully integrated power electronics, and asks two major questions based on observations of previous work:

1. Why do prototype buck converters using thin-film integrated inductors behave a certain way with respect to switching frequency?

2. Why does the hysteretic-mode, inductor-current sampling control scheme work as well as it does? Should we expect it to always work this well?

We explore both questions using data taken from an available custom front-end and custom-packaged module, focusing on really trying to explain the theoretical underpinnings for the observed behavior. We take this tack specifically because the space of thin-film inductor-based buck converters is new and exciting, and many significant products have already arisen, but exploration without mindful consideration of the results we see cannot be the most efficient way to make breakthroughs in the field.

To the first question, we suggest that the significantly worse core losses in the currently available materials refute the traditional wisdom that core losses need not be closely considered in non-isolated DC-DC converters. Rather, the focus must be on the core losses from the start, and the notions of which switching frequencies are a) relevant and b) acceptable must be re-centered.
accordingly. Upon initial presentation of raw data to our collaborators, there was a great deal of confusion as to how these results could be possible; hopefully, the discussions in chapter 1 and 3 will clear up any remaining doubt!

To the second question, we abstract out the hysteretic nature of the controller and consider the circuit using the powerful framework of sliding-mode control theory. We demonstrate from first principles that the inductor-current-sampling bang-bang architecture is indeed asymptotically stable, and investigate the theoretical underpinnings of a solution that trades off transient performance very close to the target output voltage for fixed-frequency operation.

**Future Work**

Future work in this field has two major thrusts: the first, most practical one, is continued development towards high-efficiency, high-performance fully integrated voltage converters. Enabling this is truly a question of inductor development. The conclusions in this work concern behavior *when core losses are significant* – already, we have assumed something undesirable about the inductors we are using! Ultimately, continued material development and improvement is fundamental to the next major breakthroughs in this field. Moving to extremely aggressive technologies to decrease switch charging losses and enable higher frequency operation to push down core losses may allow the designer to eke out that extra performance boost necessary to meet specifications, but at the heart of it, the inductors are the albatross around the neck of the integrated switched-inductor buck converter designer.

Soft-switching resonant or quasi-resonant topologies may also offer a significantly more attractive way out: the architectural changes reduce the high-frequency ripple content, which simultaneously decrease the core losses and the requirements on the inductance value – both major wins for thin-film inductor technologies! The steep learning curve may ultimately be
preferable to pulling one's hair out dealing with the deleterious effects of high inductor current harmonic content in the buck converter.

The second thrust is that of the continued development of theory surrounding these control paradigms, and a discussion of potential work in this direction is significantly fuzzier. At this point, interest in theory is largely relegated to mathematicians; gone are the days when circuit designers had strong grasps of control theory and network analysis. Increasing the exchange of information and ideas between system theorists and circuit designers can only increase the quality of the systems developed by circuit designers! However, it is ever the case that the designers of practical systems lead the development of the theory significantly.

With the availability of significant digital processing power in heavily scaled technologies, the ideas promulgated by system theorists regarding, e.g., higher-order sliding-mode control or model predictive control for switching systems is a large, yet unexplored space for circuit designers. There have not yet been significant demonstrations of fully-integrated controllers using these control methods, implemented by seasoned circuit designers, and one can only look forward to seeing more of these in the future.

Ultimately, the final conclusion we set forth is that we look forward to a complexity-dominated future: no more easy inductor development or circuit development is left to us, but we have now access to technologies and design frameworks that allow for unparalleled deployment of increasingly architecturally complex, high-performance power distribution and management systems. These are the systems that will be necessary to supply the ultra-high-performance processors of the future.
Bibliography


